Technologic SYSTEMS

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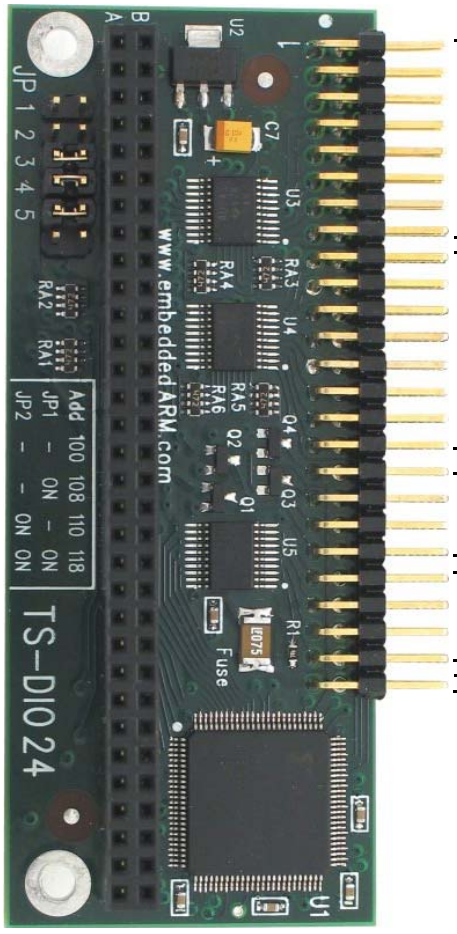
Getting started with the TS-DIO24

The TS-DIO24 is an 8-bit PC/104 expansion board that provides 24 digital I/O points. The I/O connector is an Opto-22 compatible interface that provides 16 I/O points configurable as input or output (24 mA as outputs) as well as 4 dedicated outputs capable of driving 48 mA and 4 dedicated outputs capable of sinking 1 Amp. The PC/104 interface decodes as registers in I/O space, the address is jumper selectable.

- 24 Digital I/O points
- Opto-22 compatible 50 pin connector
- 4 dedicated 48 mA ouputs, 4 dedicated 1 Amp outputs
- 16 programmable I/O points
- I/O address jumper selectable
- 4 interrupt capable inputs



50 pin connector pin out and electrical ratings

I/O Point Name	I/O Pin #	Ground Pin #	Signal Type
C7	1	2	**Port C** **Input:** TTL input (4.7k Ω pullup to +5vdc) (bits0-3 interrupt capable) **Output:** 24 mA output (0-5V output drive)
C6	3	4	
C5	5	6	
C4	7	8	
C3	9	10	
C2	11	12	
C1	13	14	
C0	15	16	
B7	17	18	**Port B** **Input:** TTL input (4.7k Ω pullup to +5V) **Output:** 24 mA output (0-5V output drive)
B6	19	20	
B5	21	22	
B4	23	24	
B3	25	26	
B2	27	28	
B1	29	30	
B0	31	32	
A7	33	34	**Port A** **Output only:** 1 Amp sink (open-drain 30V tolerant)
A6	35	36	
A5	37	38	
A4	39	41	
A3	41	43	**Port A** **Output only:** 48 mA output (0-5V output drive)
A2	43	45	
A1	45	47	
A0	47	48	
5V power	49	50	**Auxiliary power** protected by 750 mA Poly-Fuse

Transient suppression diodes required when driving inductive loads.

Register map

I/O Address	Description	Data	Bits and such
BASE + 0	Board Identifier	ASCII 'T' (RO)	ASCII 'T' equals hex 0x54
BASE + 1	reserved		
BASE + 2	Jumper status	(RO)	**Bit 0:** Jumper 1 ('1'=on, '0'=off) **Bit 1:** Jumper 2 ('1'=on, '0'=off) **Bit 2:** Jumper 3 ('1'=on, '0'=off) **Bit 3:** Jumper 4 ('1'=on, '0'=off) **Bit 4:** Jumper 5 ('1'=on, '0'=off)
BASE + 3	Interrupt Control Register	(R/W)	**Bit 0:** PortC bit 0 connects to IRQ5 **Bit 1:** PortC bit 1 connects to IRQ6 **Bit 2:** PortC bit 2 connects to IRQ7 **Bit 3:** PortC bit 3 connects to IRQ9 **Bit 4:** IRQ5 polarity is inverted **Bit 5:** IRQ6 polarity is inverted **Bit 6:** IRQ7 polarity is inverted **Bit 7:** IRQ9 polarity is inverted (Bits 4-7, '1'=invert, '0'=normal, reset='0')
BASE + 4	Data Direction Register	(R/W)	**Bit 0:** PortC direction ('1'=output, '0'=input, reset='0') **Bit 1:** PortB direction ('1'=output, '0'=input, reset='0') **Bit 2:** PortA direction ('1'=output, '0'=input, reset='0') (The reset condition of the Data Direction Register will reflect the state of jumpers JP3-5 at power up, changes written to the DDR will override the function selected by the jumpers) **Bits 3-6:** reserved **Bit 7:** IRQ sharing ('1'=enabled, '0'=disabled, reset='0') (IRQ sharing can only be used with products using the ARM architecture. When IRQ sharing is enabled IRQs are tri-stated when not asserted)
BASE + 5	Port A Data Register	(R/W)	Bits 0-7 correspond to PortA pins 0-7
BASE + 6	Port B Data Register	(R/W)	Bits 0-7 correspond to PortB pins 0-7
BASE + 7	Port C Data Register	(R/W)	Bits 0-7 correspond to PortC pins 0-7

Jumper settings for base address selection

X86 I/O address	JP2	JP1
0x100	off	off
0x108	off	on
0x110	off	on
0x118	on	on

Jumper settings for direction, ports A & B

Jumper	OFF	ON
JP3	Port A outputs	Port A inputs
JP4	Port B outputs	Port B inputs

Jumper settings for port C reset state

Jumper	OFF	ON
JP5	Outputs set to '0'	Outputs set to '1'