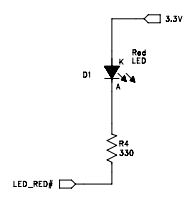
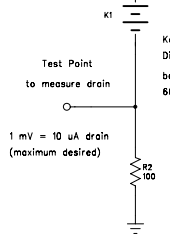
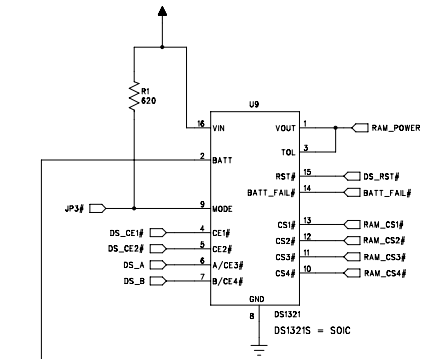
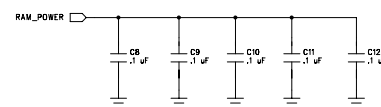
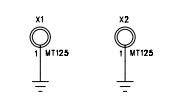
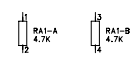
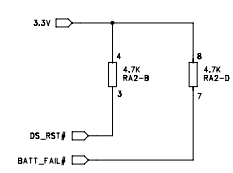
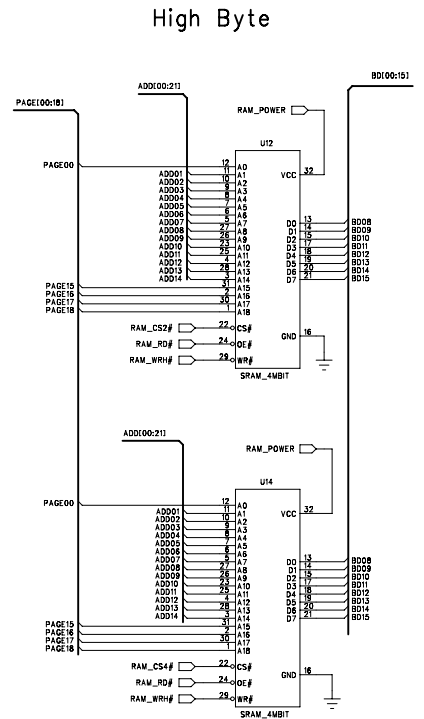
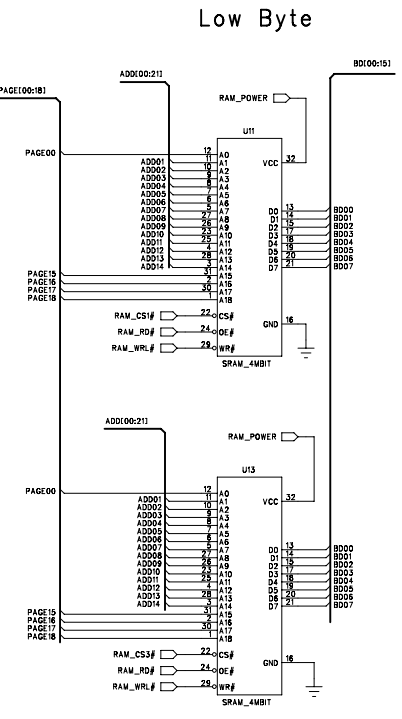
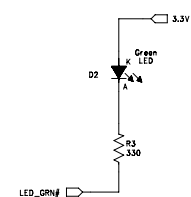


Technologic Systems	Date	Sept. 13, 2005
Title:	TS-NVRAM2 PC/104, PLD	
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TOL tied to Vout -
Reset trip is 4.25 to 4.50 V
This is also when the battery
is switched in or out

Mode = GND at power up --> 8-bit mode
Mode = Vout at power up --> 16-bit mode



Technologic Systems	Date Sept. 13, 2005
Title: TS-NVRAM2 RAM, Battery, DS1321	
Rev: 1.0	Designer RLM Sheet 2 of 2