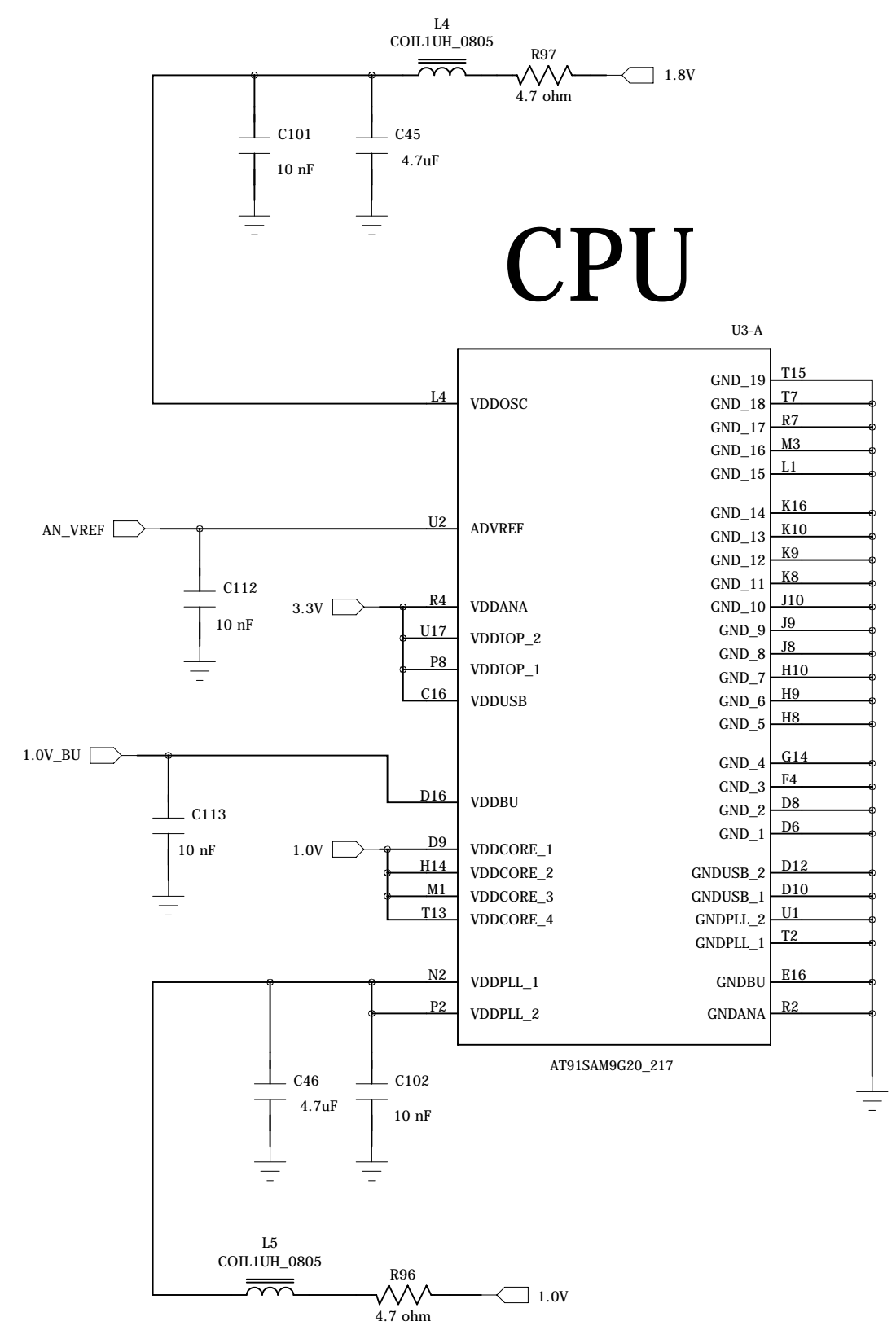


# CPU

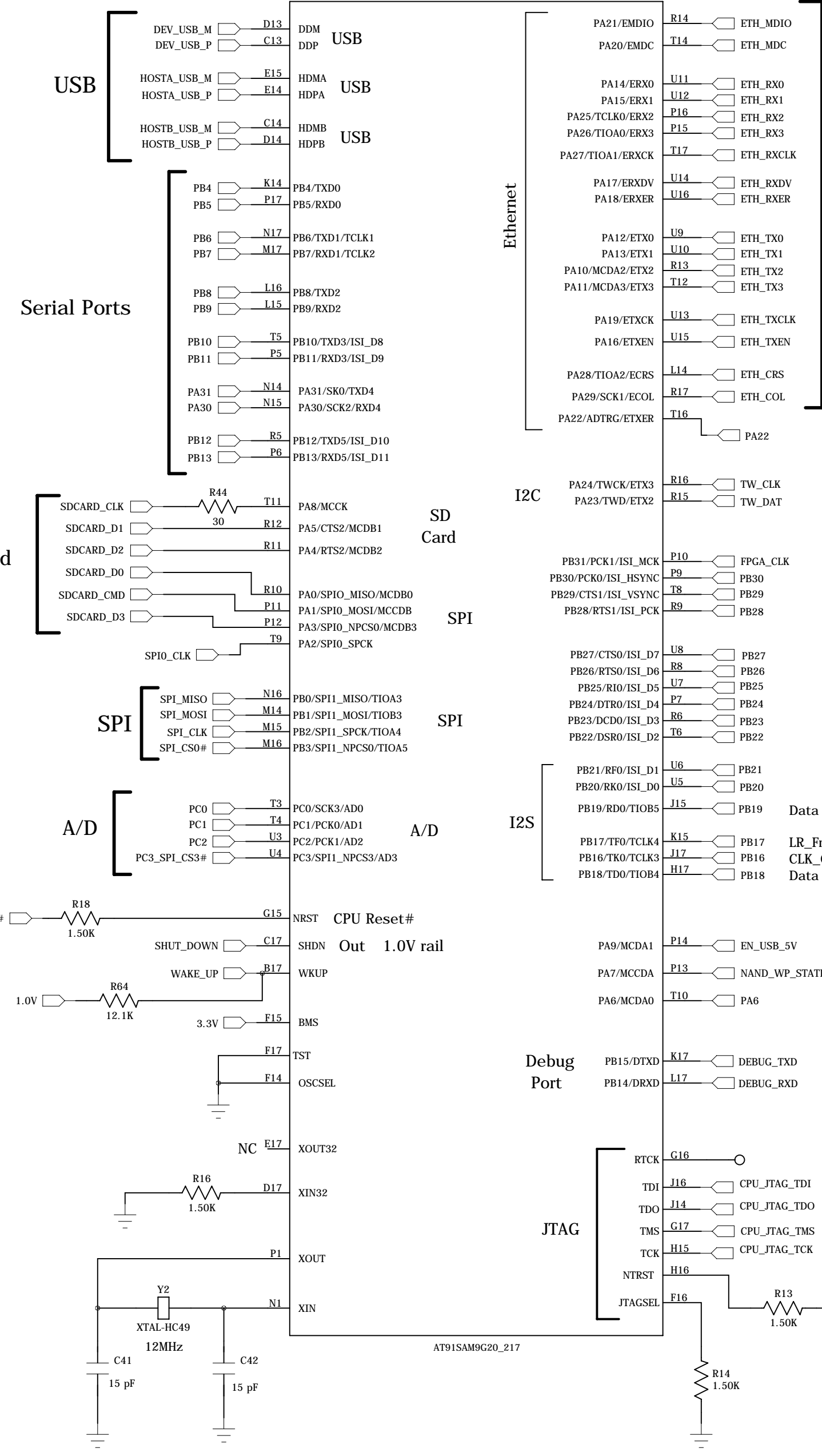
U3-C



# CPU

U3-A

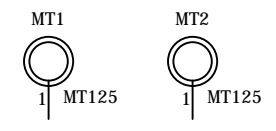
**CPU\_RESET#**  
is bi-directional and  
can be programmed  
to cause interrupt  
instead of reset



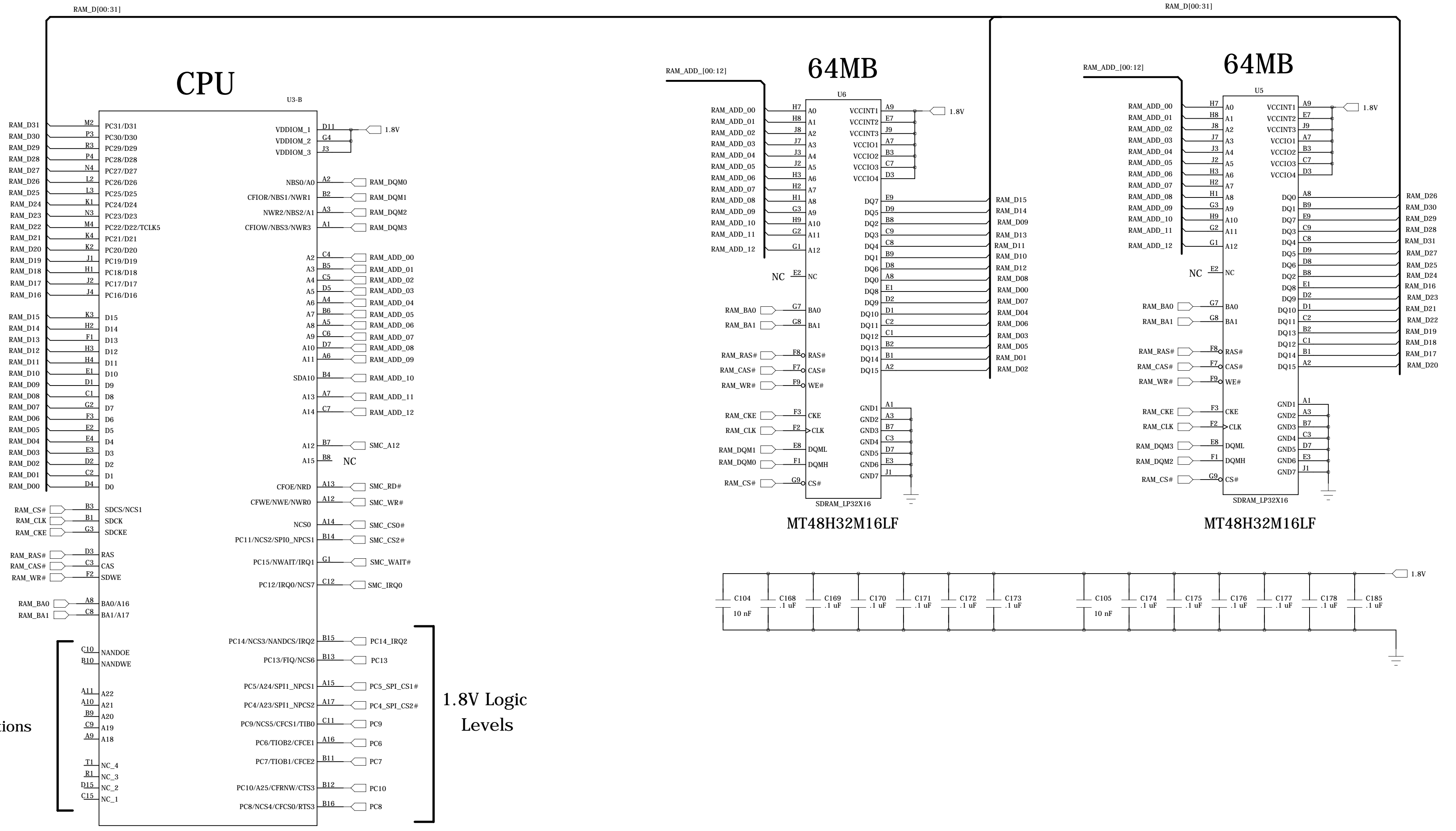
To Ethernet  
PHY

To DAC

Suggest PA6 = En\_Power to RS-232 Transceivers



# 128 MB RAM



No Connections

1.8V Logic Levels

Logic Levels in this "Gate" are all 0 to 1.8V

A3P125 has:  
 3000 Tiles (about 1200 LUTs)  
 4 Kbytes total of Block RAM  
 97 I/O with 144 pin package  
 "true instant ON"  
 Input PLL clock = 1.5 MHz min

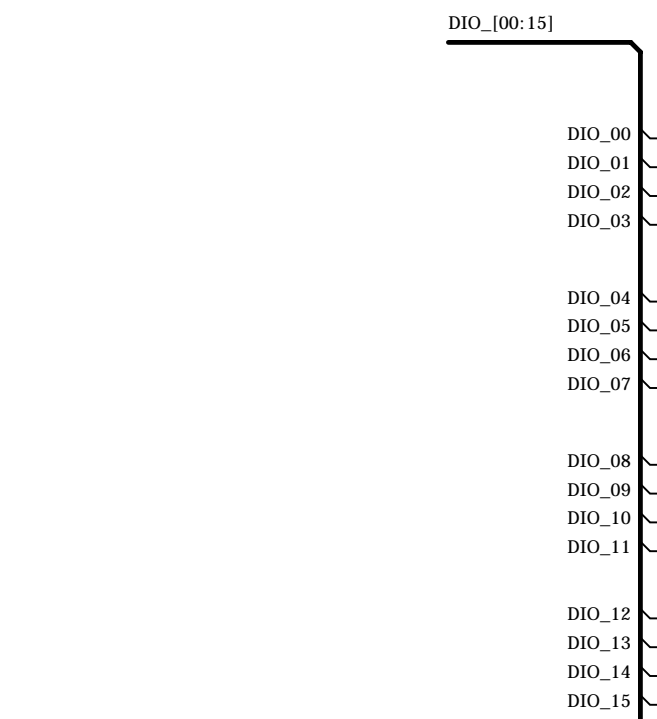
# FPGA

Warning: MUX\_AD00 thru AD07 is used by NAND Flash

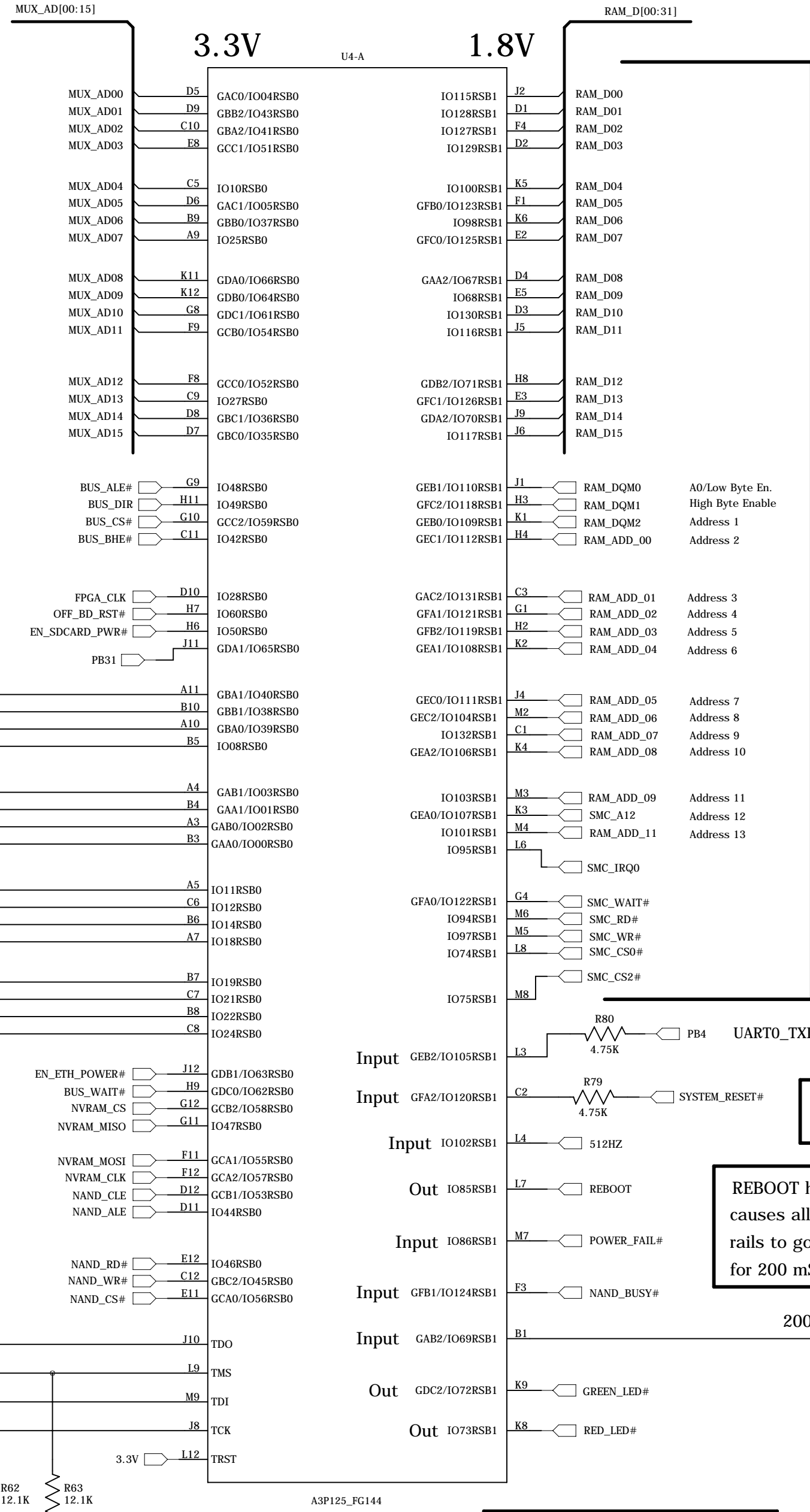
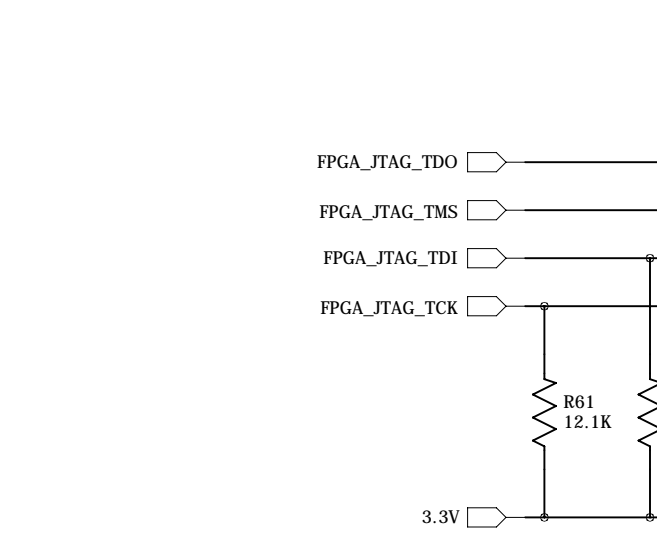
Devices connected to this bus must never drive it when BUS\_RD# is deasserted (must be off within 30 nS of deassertion)

Devices must pull the BUS\_WAIT# line low if they need more than 150 nS strobe

FPGA\_CLK = CPU Timer Out



All NVRAM interface signals must be kept in low state when not accessing NVRAM



When SYSTEM\_RESET# asserted, then set these as follows:

Asserted:  
 OFF\_BD\_RST#  
 EN\_SDCARD\_PWR#  
 RED\_LED#  
 GREEN\_LED#

Deasserted:  
 EN\_ETH\_PWR#  
 REBOOT  
 NVRAM\_CS  
 NAND\_CS#

When SYSTEM\_RESET# deasserted, Latch BUS\_ALE# and BUS\_RD# into a register

Early Boot code should deassert OFF\_BD\_RST# signal. (after SPI Flash loaded into RAM)

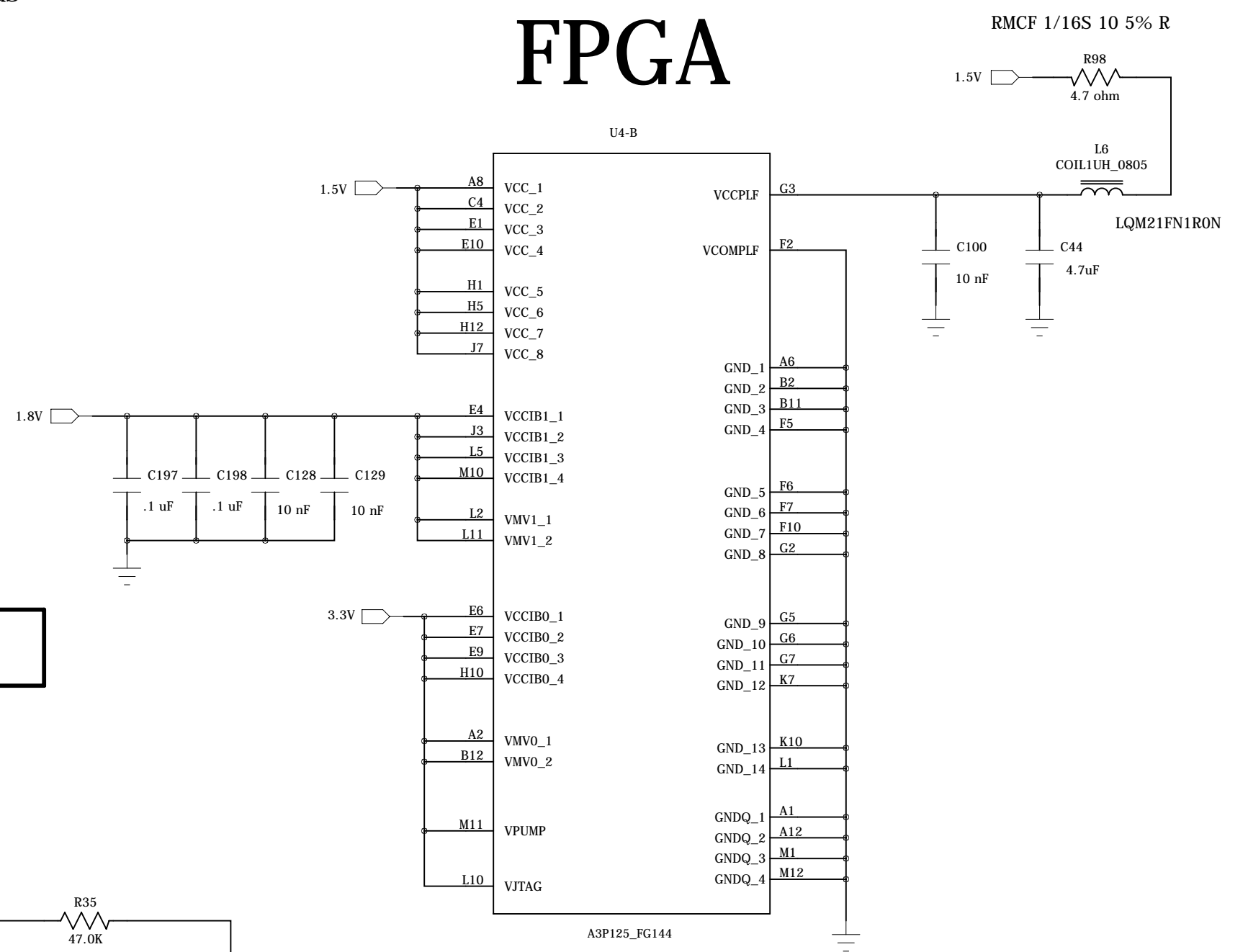
## Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS\_ALE# = MODE1  
 BUS\_RD# = MODE2

To CPU Address/Data Bus

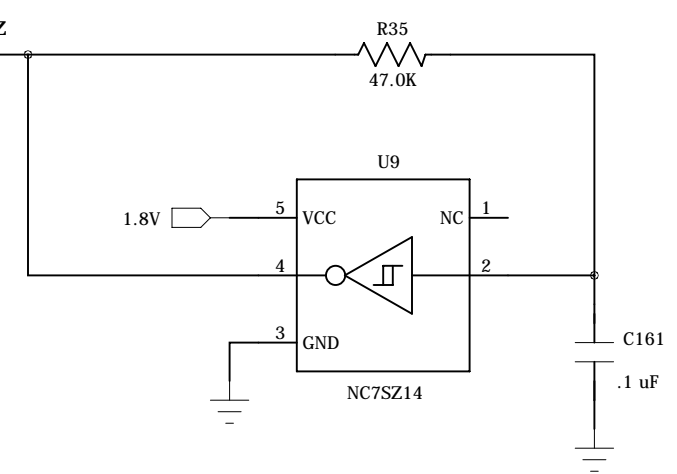
# FPGA



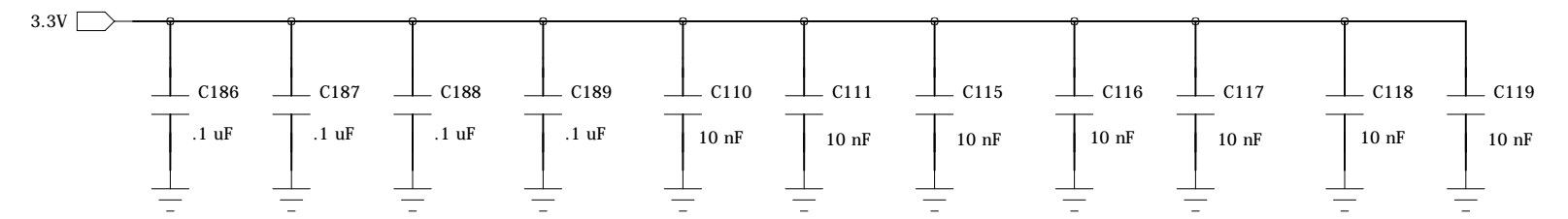
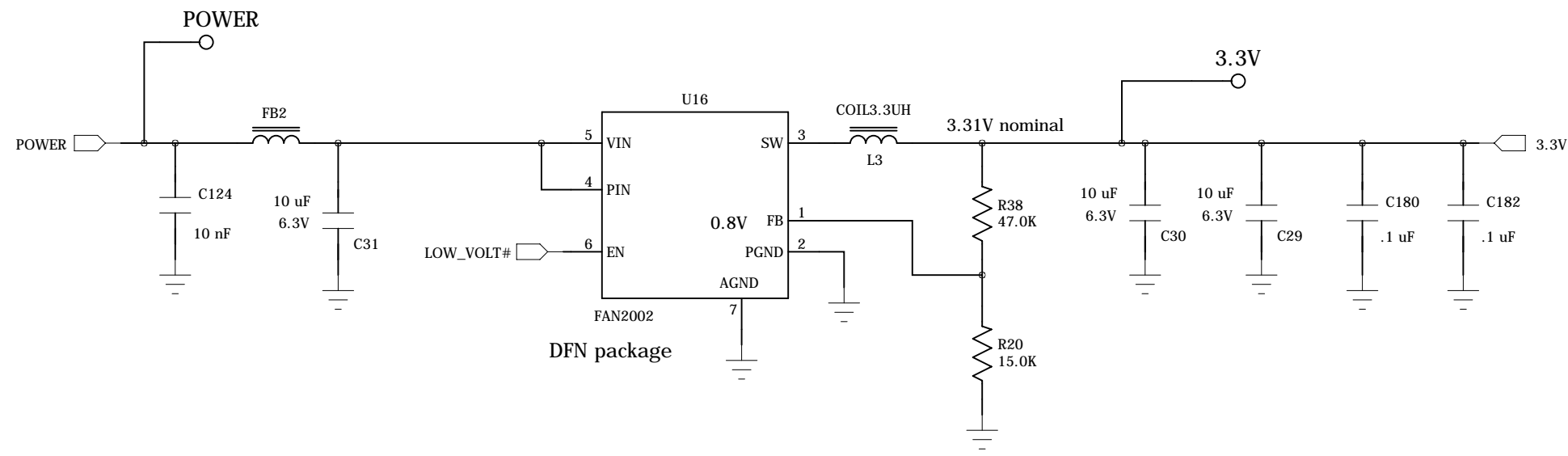
Inputs with 1.8V rail have diode clamp to 1.8V

REBOOT high causes all power rails to go low for 200 mS

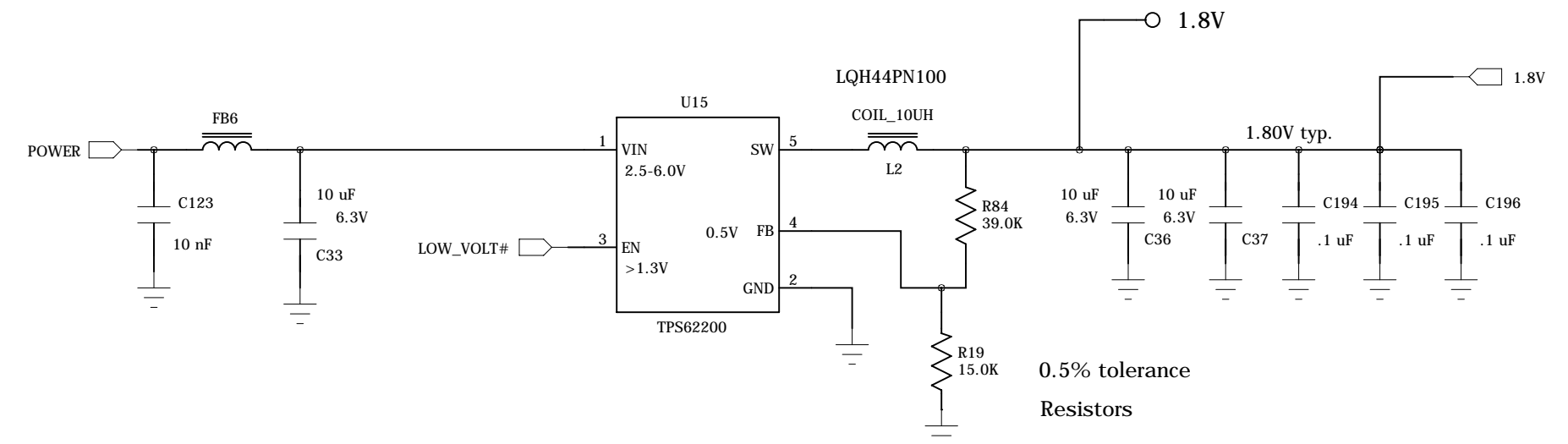
RED\_LED# and GREEN\_LED# must be Open Drain



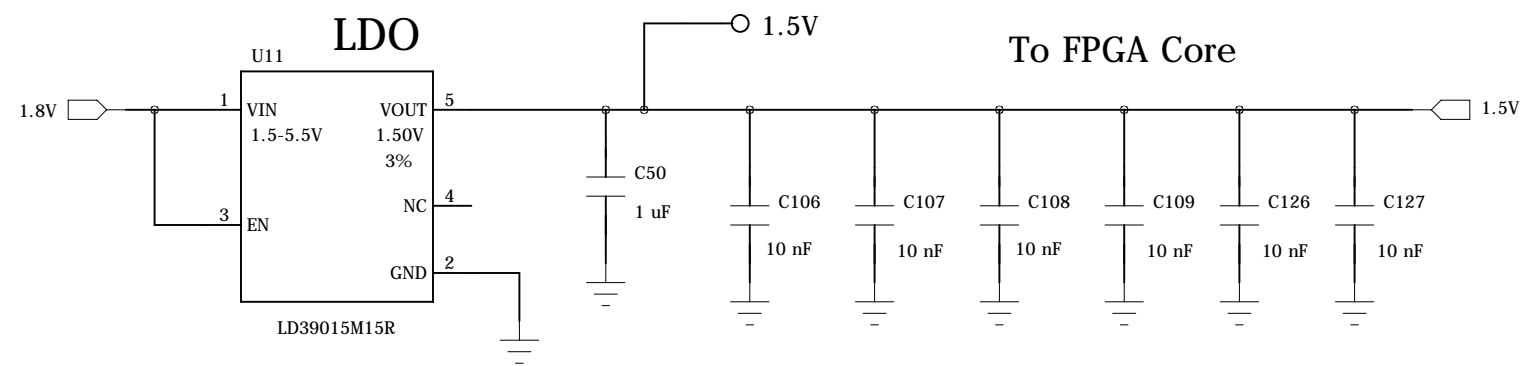
# 3.3V Supply



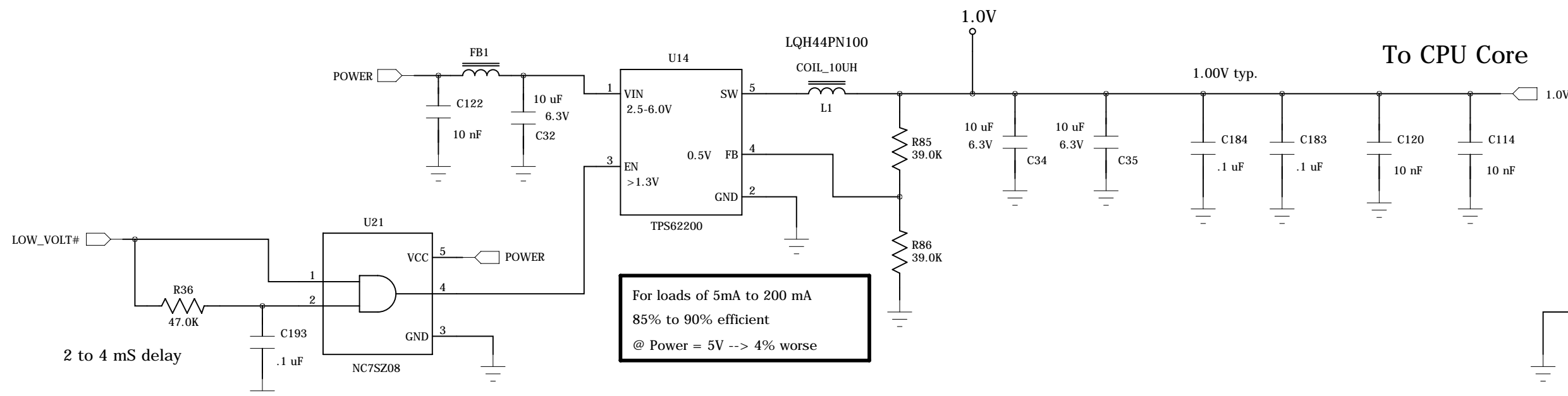
# 1.8V Supply



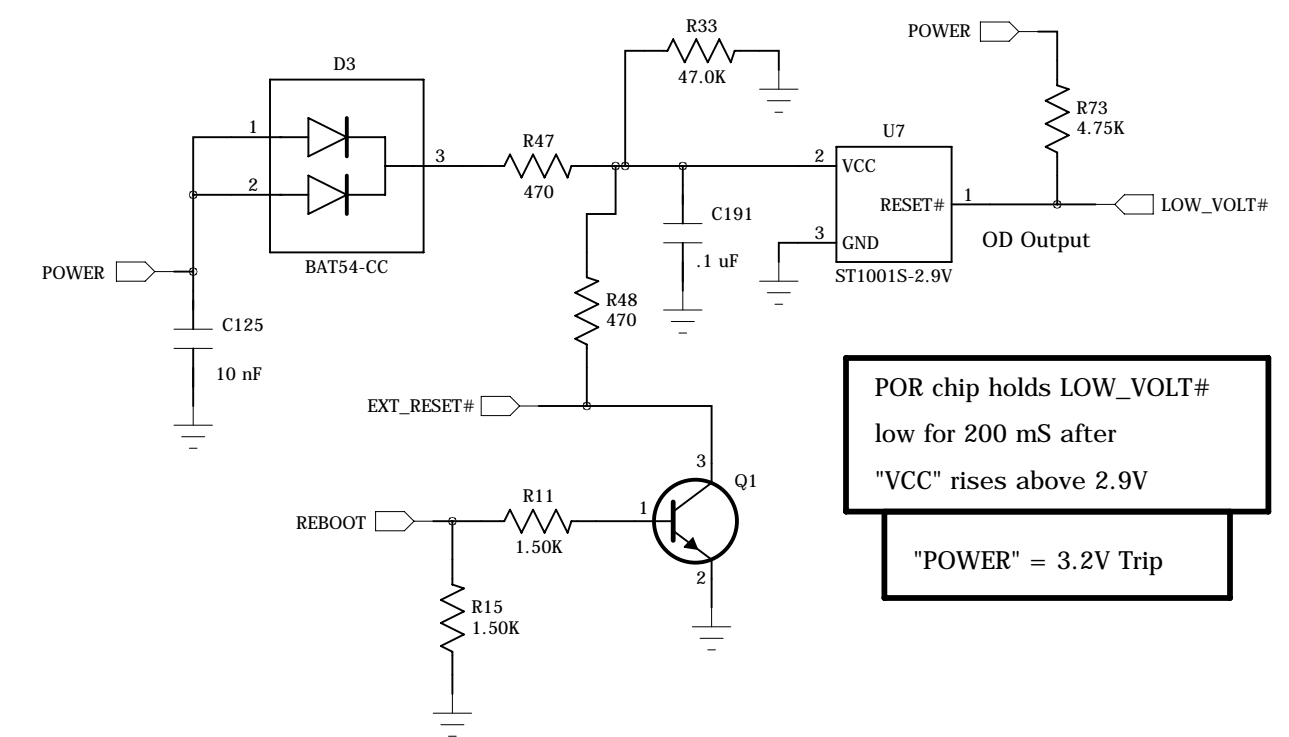
# 1.5V Supply



# 1.0V Supply



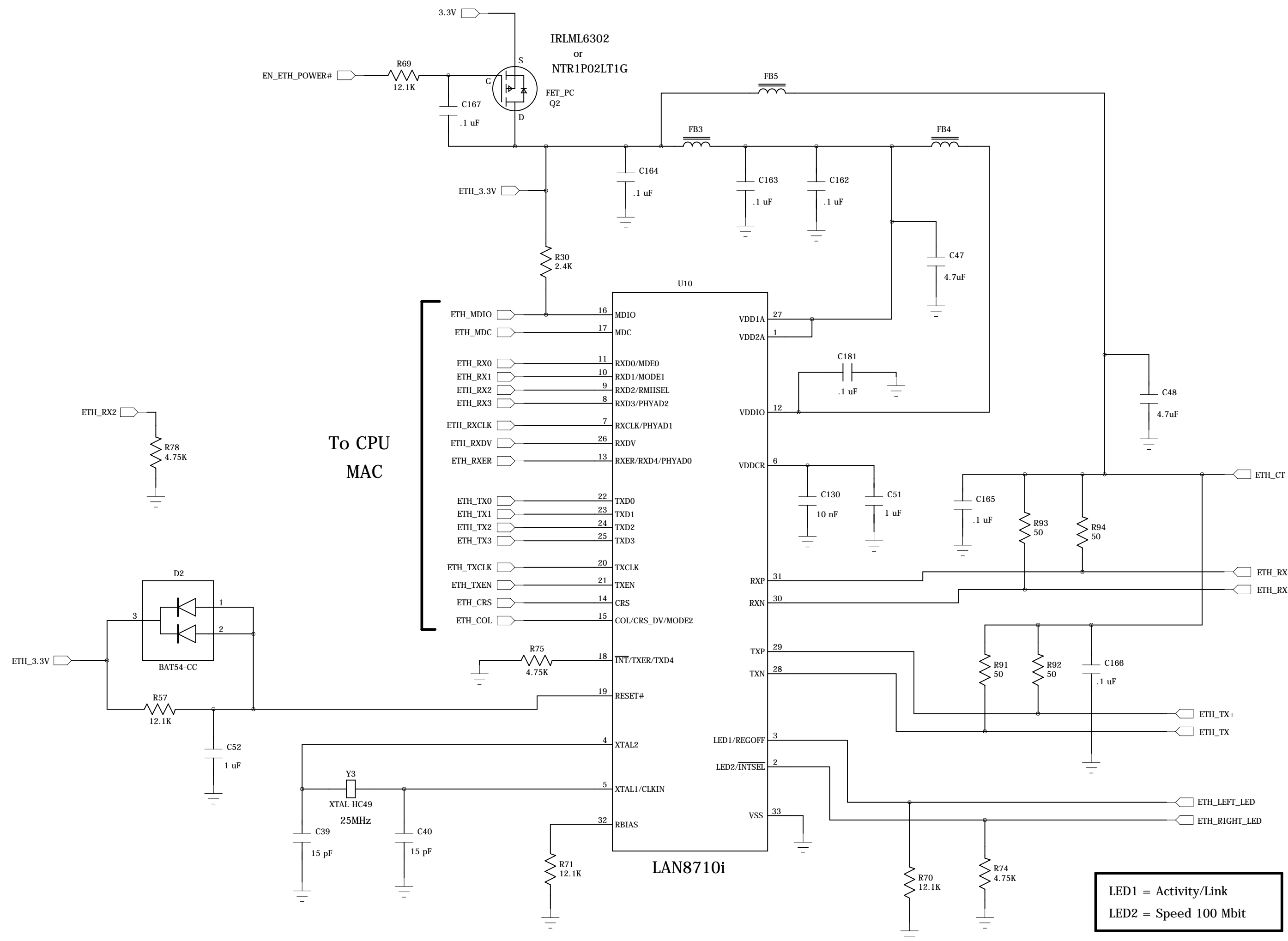
# POR



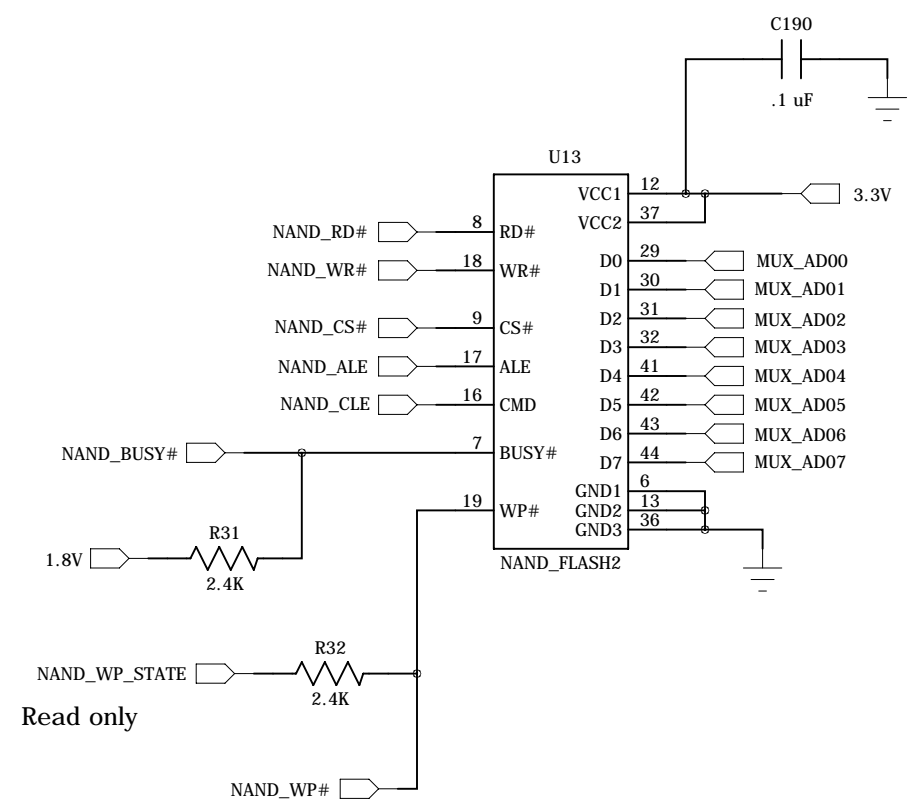
POR chip holds LOW\_VOLT# low for 200 mS after "VCC" rises above 2.9V

"POWER" = 3.2V Trip

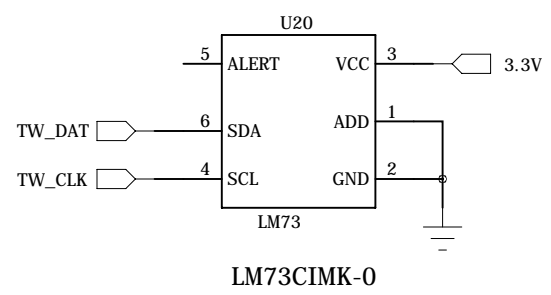
# 10/100 Ethernet



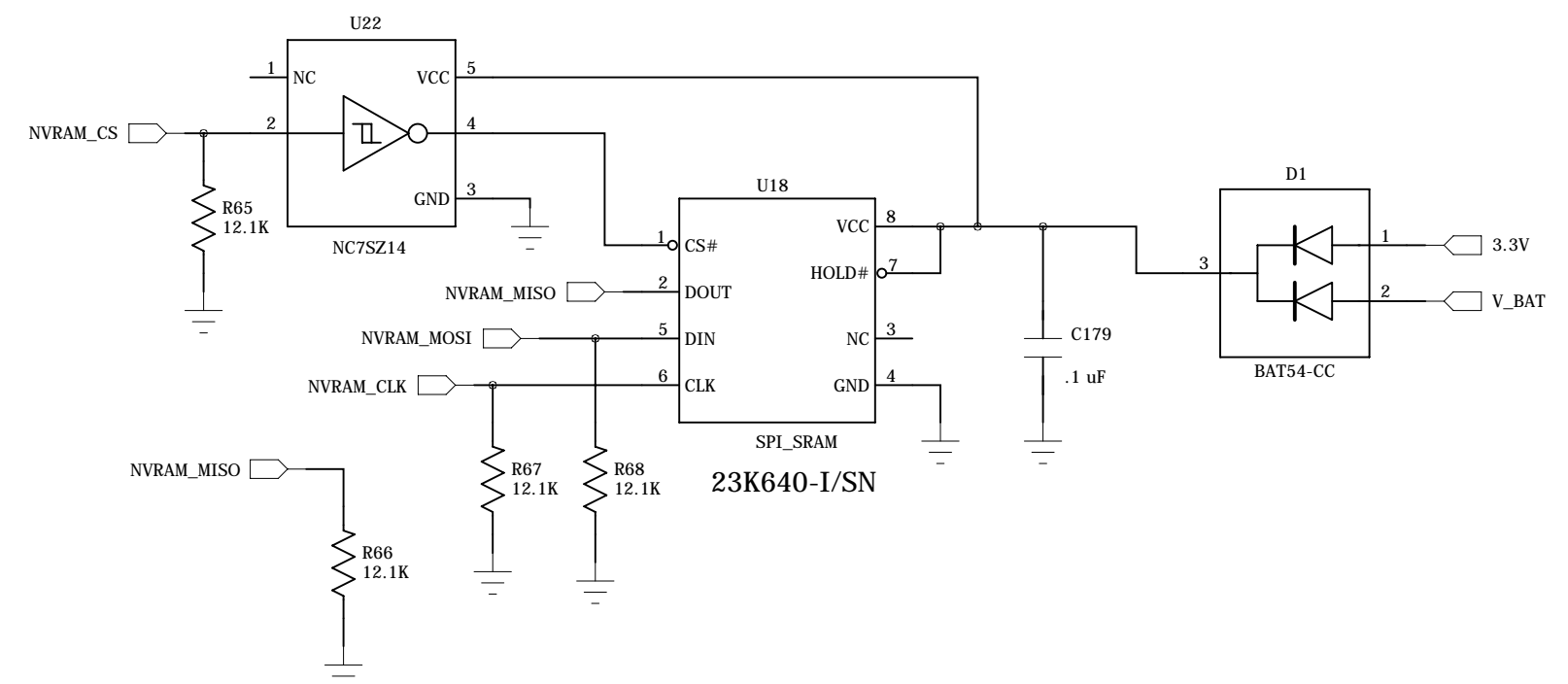
# 512 MB or 2 GB NAND Flash



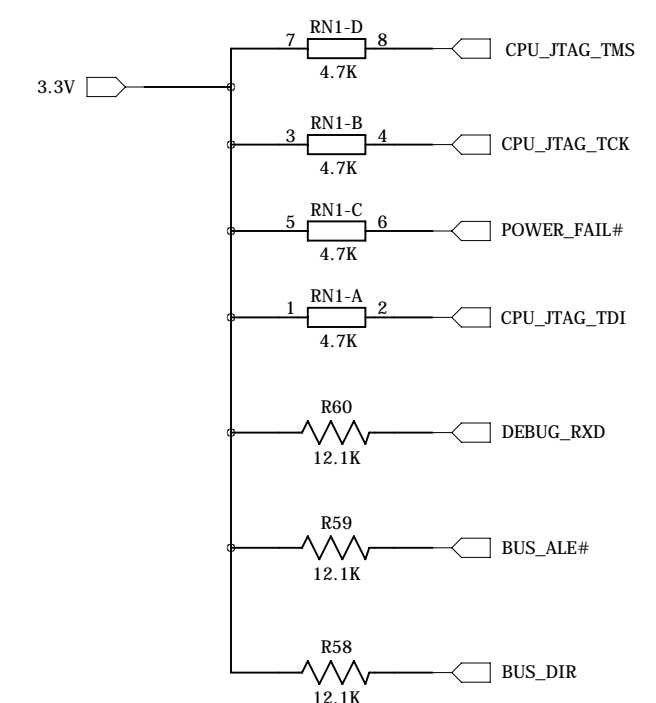
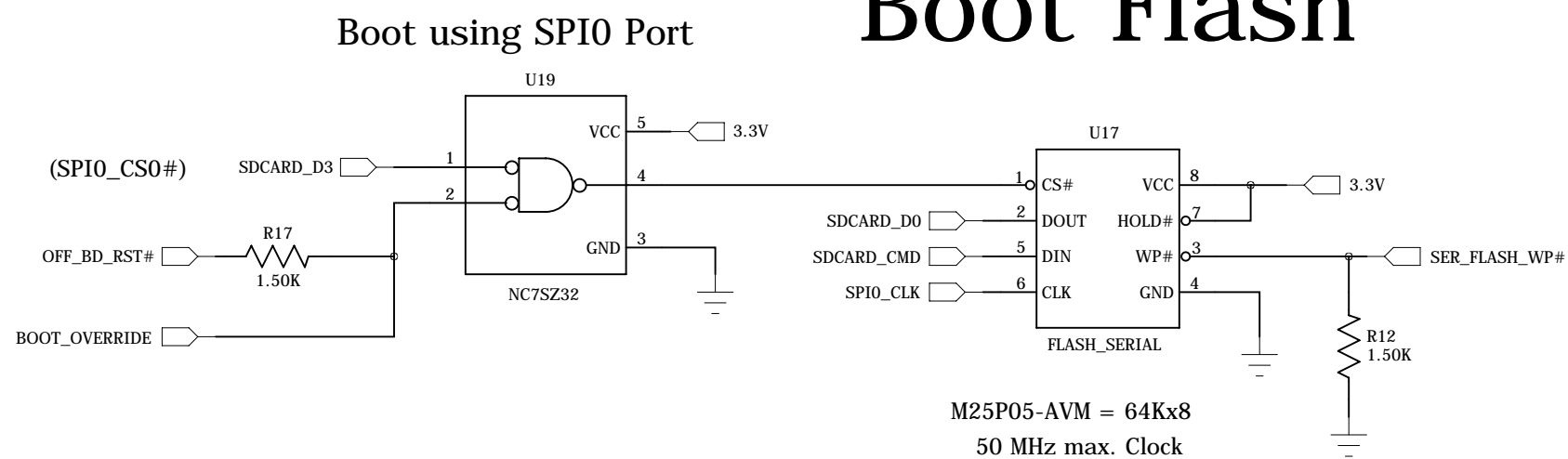
# Temp Sensor



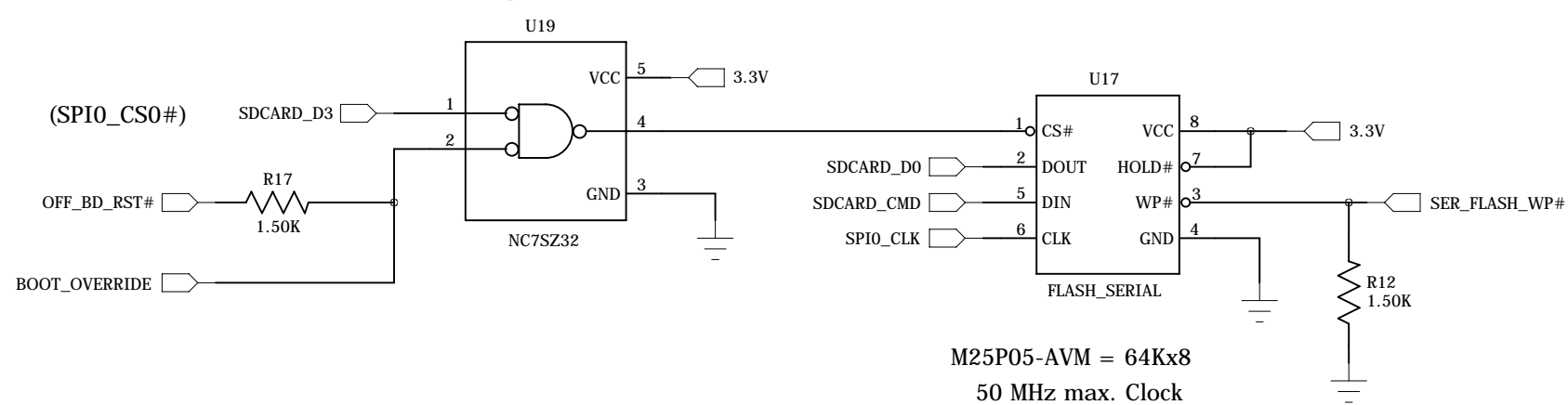
# 8K Byte NVRAM



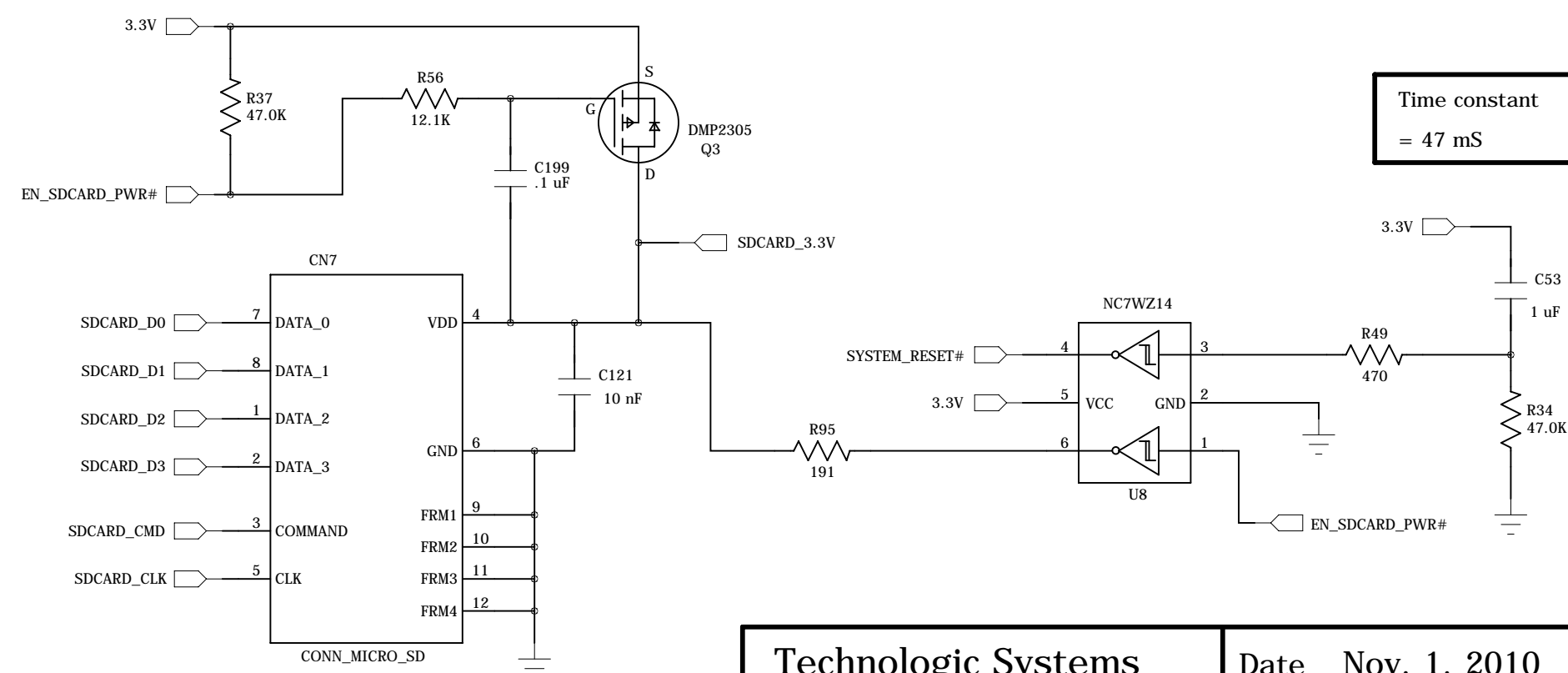
# 64KB Serial Boot Flash



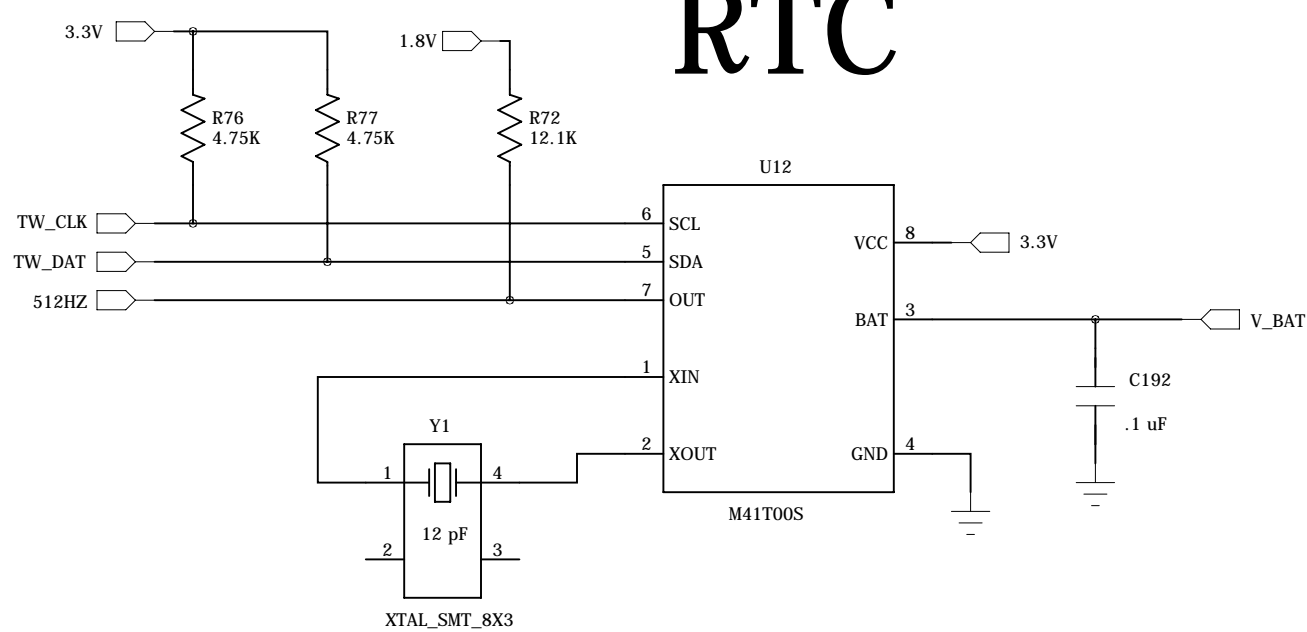
# Boot using SPI0 Port



# Micro SD Card Socket



# RTC



# Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module  
Apply 3.6V to 5.5V to these pins

Current drain is 50mA to 400 mA

EXT\_RESET# is an Input  
used to reboot the CPU

CN2 pin 27 should be connected  
to CN2 pin 33 on the base board

OFF\_BD\_RESET# is an Output  
used to reset all peripherals

POWER\_FAIL# must  
not be driven high

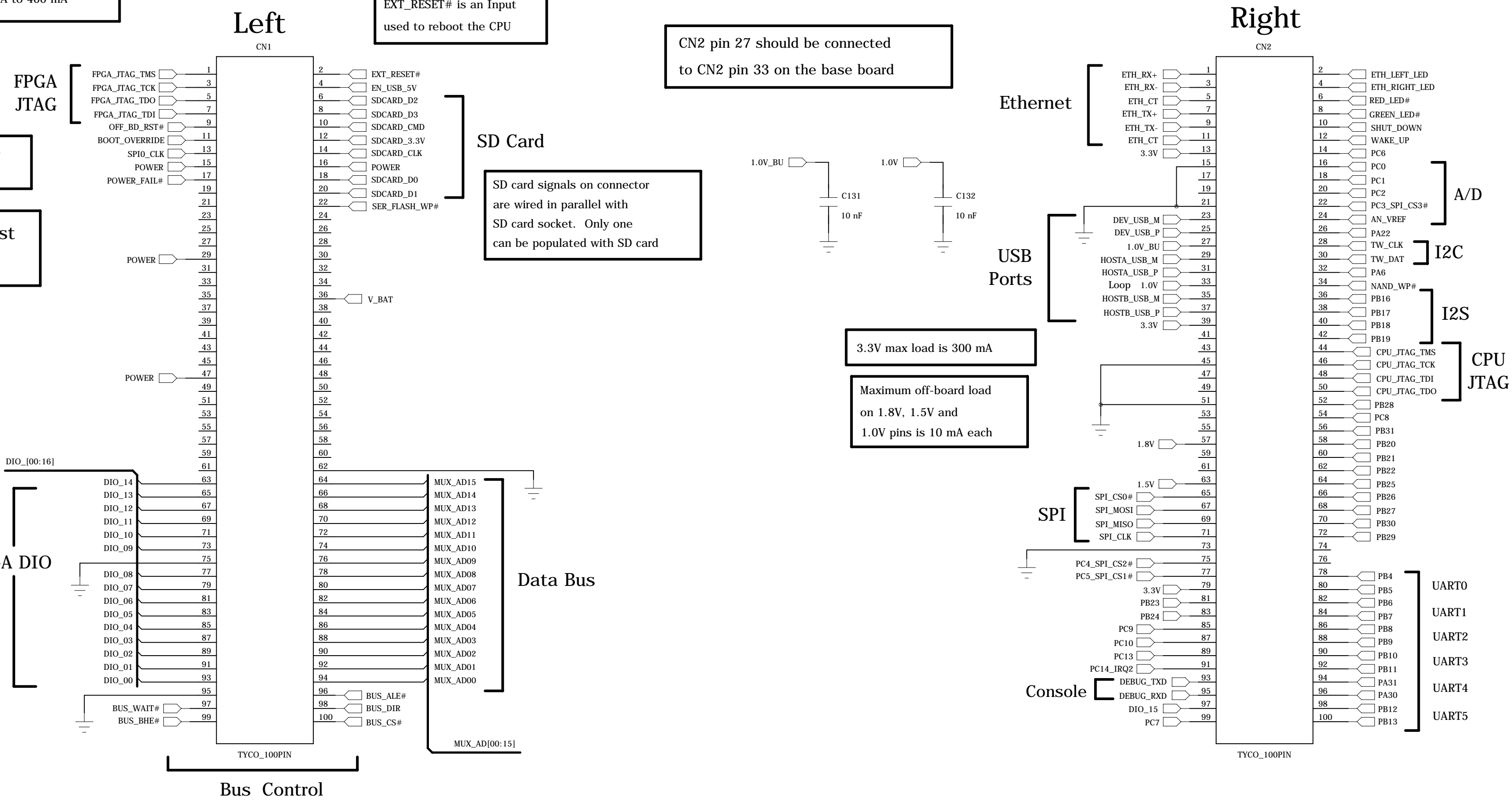
SD Card  
SD card signals on connector  
are wired in parallel with  
SD card socket. Only one  
can be populated with SD card

3.3V max load is 300 mA

Maximum off-board load  
on 1.8V, 1.5V and  
1.0V pins is 10 mA each

These DIO have 1.8V levels  
PC4, PC5, PC6  
PC7, PC8, PC9  
PC10, PC13, PC14

All other DIO uses 3.3V levels



## Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS\_DIR = MODE2

MODE1 and MODE2 states  
are latched prior to  
OFF\_BD\_RESET# deasserted

MODE1 and MODE2  
have PU resistors

Use 1.5K ohm resistor  
to "OFF\_BD\_RESET#"  
to set Mode pins "low"

Devices connected to this bus must never  
drive it when BUS\_CS# is deasserted  
(must be off within 30 nS of deassertion)

Devices must pull the BUS\_WAIT# line low  
if they need more than 150 nS strobe

The data bus can not have more than  
30 pF of off-board capacitive loading  
May need data buffer chip for heavy loads

If Bus is not needed, the following  
can be changed to DIO:  
- Bus Control signals  
- MUX\_AD08 thru 15

BUS\_ALE# = Address Latch Enable  
BUS\_BHE# = Byte High Enable (for 16-bit cycles)