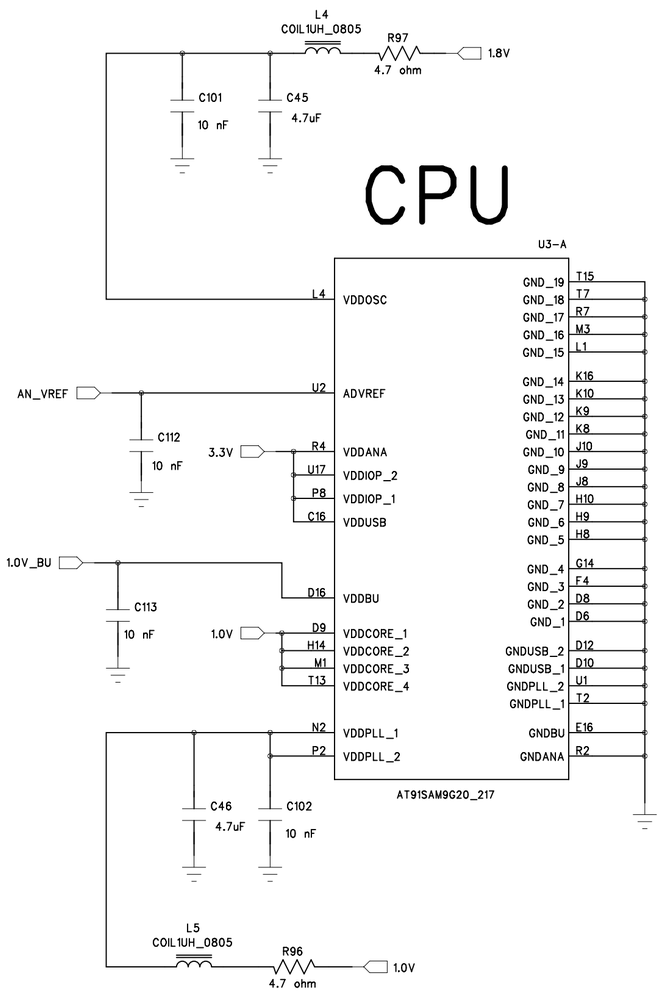
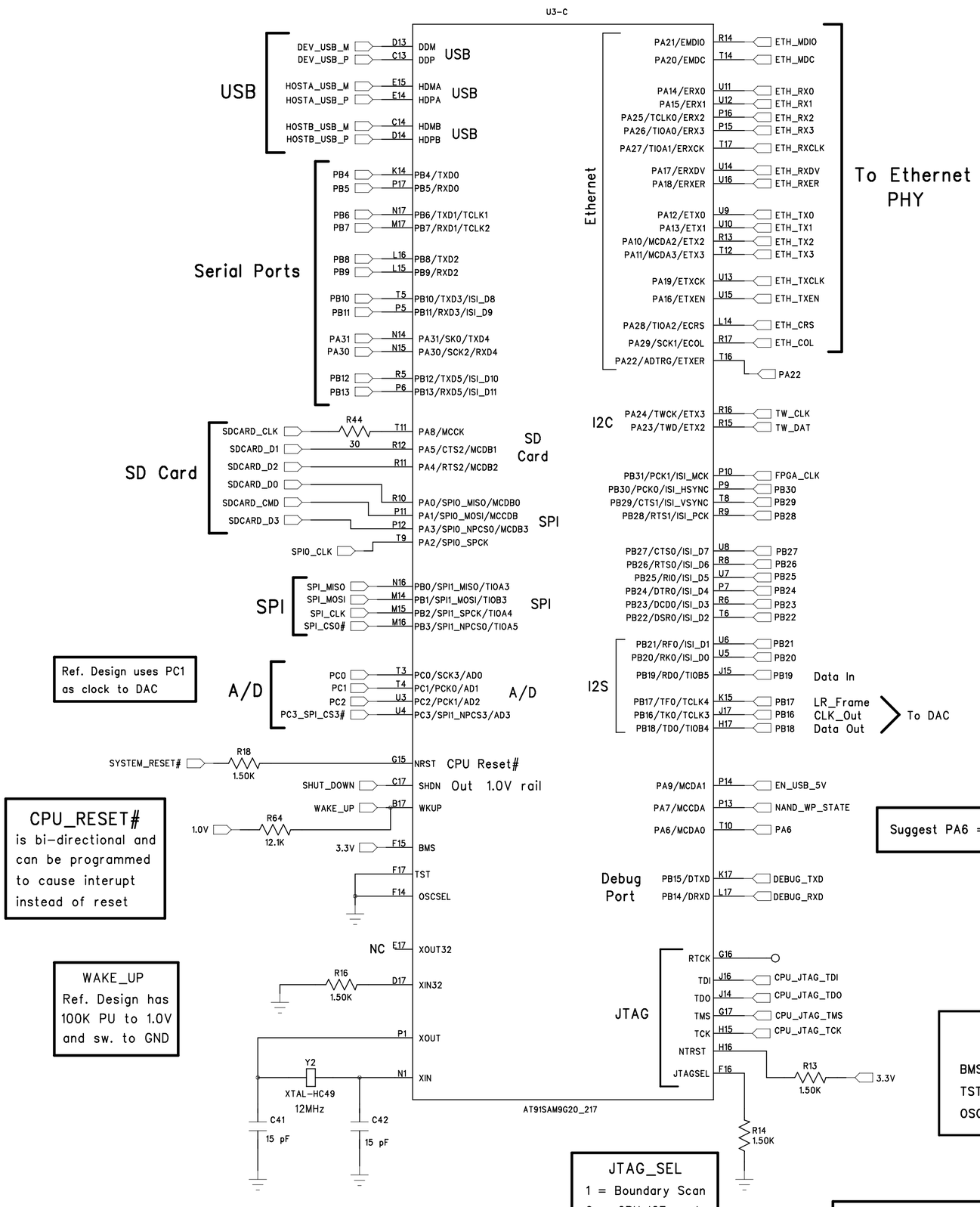
TS-4200 Rev B

CPU



CPU

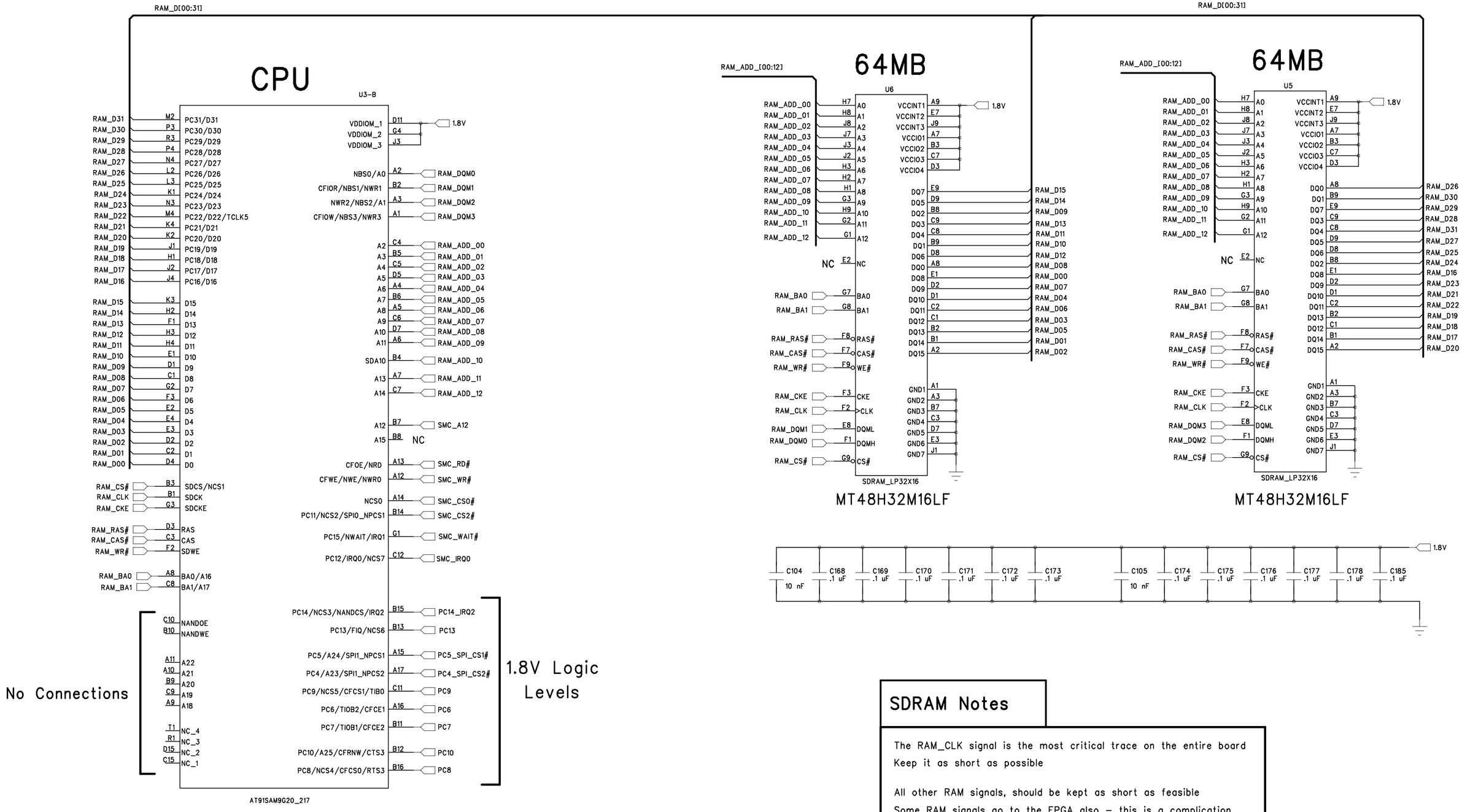


MT1 1 MT125

MT2 1 MT125

Technologic Systems	Date March 15, 2010	
Title: TS-4200 CPU		
Rev:	Designer	Sheet 1 of 7

128 MB RAM



Logic Levels in this "Gate" are all 0 to 1.8V

SDRAM Notes

The RAM_CLK signal is the most critical trace on the entire board
Keep it as short as possible

All other RAM signals, should be kept as short as feasible
Some RAM signals go to the FPGA also – this is a complication

RAM data signals can be swapped bit-wise or byte-wise
For example, D16-D23 can be swapped with D24-D31
This would require the respective DQMx lines to be swapped as well

Bit-wise swaps are allowed within a byte
For example, D2 and D5 can be swapped

Technologic Systems		Date March 15, 2010
Title: TS-4200 RAM		
Rev:	Designer RLM	Sheet 2 of 7

FPGA

A3P125 has:
3000 Tiles (about 1200 LUTs)
4 Kbytes total of Block RAM
97 I/O with 144 pin package
"true instant ON"
Input PLL clock = 1.5 MHz min

When SYSTEM_RESET# asserted, then set these as follows:

Asserted:
- OFF_BD_RST#
- EN_SDCARD_PWR#
- RED_LED#
- GREEN_LED#

Deasserted:
- EN_ETH_PWR#
- REBOOT
- NVRAM_CS
- NAND_CS#

When SYSTEM_RESET# deasserted, Latch BUS_ALE# and BUS_RD# into a register

Early Boot code should deassert OFF_BD_RST# signal. (after SPI Flash loaded into RAM)

Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1
BUS_RD# = MODE2

Warning: MUX_AD00 thru AD07 is used by NAND Flash

Devices connected to this bus must never drive it when BUS_RD# is deasserted (must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

FPGA_CLK = CPU Timer Out

DIO_00 can be BUS_IRQ
DIO_01 can be BUS_DIR
DIO_02 can be BUS_CS2#
DIO_03 can be BUS_CS3#
DIO_04 can be BUS_CS4#
DIO_05 can be BUS_CS5#

DIO_09 = Push_switch

All NVRAM interface signals must be kept in low state when not accessing NVRAM

3.3V U4-A 1.8V

MUX_AD[00:15]
MUX_AD00 D5 GAC0/IO04RSB0
MUX_AD01 D9 GBB2/IO43RSB0
MUX_AD02 C10 GBA2/IO41RSB0
MUX_AD03 E8 GCC1/IO51RSB0
MUX_AD04 C5 IO10RSB0
MUX_AD05 D6 GAC1/IO05RSB0
MUX_AD06 B9 GBB0/IO37RSB0
MUX_AD07 A9 IO25RSB0
MUX_AD08 K11 GDA0/IO66RSB0
MUX_AD09 K12 GDB0/IO64RSB0
MUX_AD10 G8 GDC1/IO61RSB0
MUX_AD11 F9 GCB0/IO54RSB0
MUX_AD12 F8 GCC0/IO52RSB0
MUX_AD13 C9 IO27RSB0
MUX_AD14 D8 GBC1/IO36RSB0
MUX_AD15 D7 GBC0/IO35RSB0

BUS_ALE# G9 IO48RSB0
BUS_RD# H11 IO49RSB0
BUS_WR# G10 GCC2/IO59RSB0
BUS_BHE# C11 IO42RSB0

FPGA_CLK D10 IO28RSB0
OFF_BD_RST# H7 IO60RSB0
EN_SDCARD_PWR# H6 IO50RSB0
PB31 J11 GDA1/IO65RSB0

DIO_[00:15]
DIO_00 A11 GBA1/IO40RSB0
DIO_01 B10 GBB1/IO38RSB0
DIO_02 A10 GBA0/IO39RSB0
DIO_03 B5 IO08RSB0
DIO_04 A4 GAB1/IO03RSB0
DIO_05 B4 GAA1/IO01RSB0
DIO_06 A3 GAB0/IO02RSB0
DIO_07 B3 GAA0/IO00RSB0
DIO_08 A5 IO11RSB0
DIO_09 C6 IO12RSB0
DIO_10 B6 IO14RSB0
DIO_11 A7 IO18RSB0
DIO_12 B7 IO19RSB0
DIO_13 C7 IO21RSB0
DIO_14 B8 IO22RSB0
DIO_15 C8 IO24RSB0

EN_ETH_POWER# J12 GDB1/IO63RSB0
BUS_WAIT# H9 GDC0/IO62RSB0
NVRAM_CS G12 GCB2/IO58RSB0
NVRAM_MISO G11 IO47RSB0
NVRAM_MOSI F11 GCA1/IO55RSB0
NVRAM_CLK F12 GCA2/IO57RSB0
NAND_CLE D12 GCB1/IO53RSB0
NAND_ALE D11 IO44RSB0
NAND_RD# E12 IO46RSB0
NAND_WR# C12 GBC2/IO45RSB0
NAND_CS# E11 GCA0/IO56RSB0

FPGA_JTAG_TDO J10 TDO
FPGA_JTAG_TMS L9 TMS
FPGA_JTAG_TDI M9 TDI
FPGA_JTAG_TCK J8 TCK
3.3V L12 TRST
R61 12.1K
R62 12.1K
R63 12.1K
3.3V

A3P125_FG144

RAM_D[00:31]
IO115RSB1 J2 RAM_D00
IO128RSB1 D1 RAM_D01
IO127RSB1 F4 RAM_D02
IO129RSB1 D2 RAM_D03
IO100RSB1 K5 RAM_D04
GFB0/IO123RSB1 F1 RAM_D05
IO98RSB1 K6 RAM_D06
GFC0/IO125RSB1 E2 RAM_D07
GAA2/IO67RSB1 D4 RAM_D08
IO68RSB1 E5 RAM_D09
IO130RSB1 D3 RAM_D10
IO116RSB1 J5 RAM_D11
GDB2/IO71RSB1 H8 RAM_D12
GFC1/IO126RSB1 E3 RAM_D13
GDA2/IO70RSB1 J9 RAM_D14
IO117RSB1 J6 RAM_D15

GEB1/IO110RSB1 J1 RAM_DQM0 A0/Low Byte En.
GFC2/IO118RSB1 H3 RAM_DQM1 High Byte Enable
GEB0/IO109RSB1 K1 RAM_DQM2 Address 1
GEC1/IO112RSB1 H4 RAM_ADD_00 Address 2
GAC2/IO131RSB1 C3 RAM_ADD_01 Address 3
GFA1/IO121RSB1 G1 RAM_ADD_02 Address 4
GFB2/IO119RSB1 H2 RAM_ADD_03 Address 5
GEA1/IO108RSB1 K2 RAM_ADD_04 Address 6
GEC0/IO111RSB1 J4 RAM_ADD_05 Address 7
GEC2/IO104RSB1 M2 RAM_ADD_06 Address 8
IO132RSB1 C1 RAM_ADD_07 Address 9
GEA2/IO106RSB1 K4 RAM_ADD_08 Address 10
IO103RSB1 M3 RAM_ADD_09 Address 11
GEA0/IO107RSB1 K3 SMC_A12 Address 12
IO101RSB1 M4 RAM_ADD_11 Address 13
IO95RSB1 L6 SMC_IRQ0
GFA0/IO122RSB1 G4 SMC_WAIT#
IO94RSB1 M6 SMC_RD#
IO97RSB1 M5 SMC_WR#
IO74RSB1 L8 SMC_CS0#
IO75RSB1 M8 SMC_CS2#

Input GEB2/IO105RSB1 L3 PB4 UART0_TXD
Input GFA2/IO120RSB1 C2 SYSTEM_RESET#
Input IO102RSB1 L4 512HZ
Out IO85RSB1 L7 REBOOT
Input IO86RSB1 M7 POWER_FAIL#
Input GFB1/IO124RSB1 F3 NAND_BUSY#
Input GAB2/IO69RSB1 B1
Out GDC2/IO72RSB1 K9 GREEN_LED#
Out IO73RSB1 K8 RED_LED#

Inputs with 1.8V rail are 3.3V tolerant

REBOOT high causes all power rails to go low for 200 mS

RED_LED# and GREEN_LED# must be Open Drain

To CPU Address/Data Bus

200 Hz
R35 47.0K
U9
1.8V 5 VCC NC 1
4 2
3 GND
NC7SZ14
C161 .1 uF

FPGA

U4-B
1.5V A8 VCC_1, C4 VCC_2, E1 VCC_3, E10 VCC_4, H1 VCC_5, H5 VCC_6, H12 VCC_7, J7 VCC_8
1.8V E4 VCCIB1_1, J3 VCCIB1_2, L5 VCCIB1_3, M10 VCCIB1_4
VMV1_1 L2, VMV1_2 L11
3.3V E6 VCCIB0_1, E7 VCCIB0_2, E9 VCCIB0_3, H10 VCCIB0_4
VMV0_1 A2, VMV0_2 B12
VPUMP M11
VJTAG L10
VCCPLF G3
VCOMPLF F2
GND_1 A6, GND_2 B2, GND_3 B11, GND_4 F5, GND_5 F6, GND_6 F7, GND_7 F10, GND_8 G2, GND_9 G5, GND_10 G6, GND_11 G7, GND_12 K7, GND_13 K10, GND_14 L1
GNDQ_1 A1, GNDQ_2 A12, GNDQ_3 M1, GNDQ_4 M12

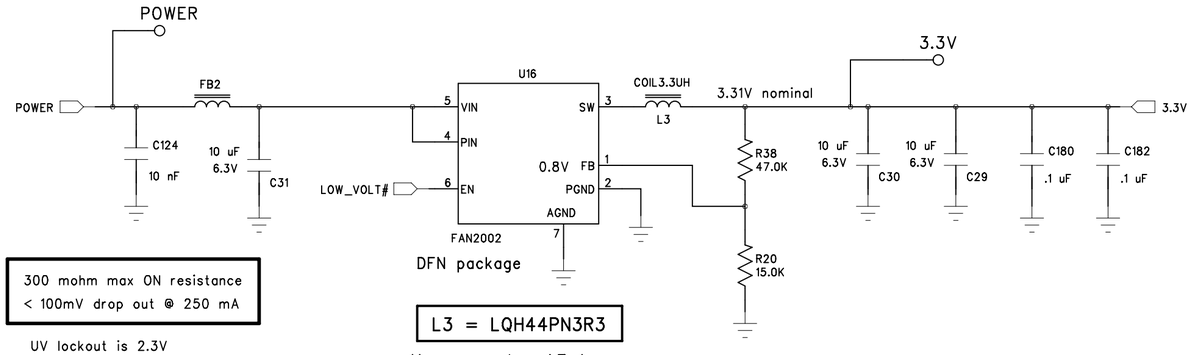
C197 .1 uF, C198 .1 uF, C128 10 nF, C129 10 nF

A3P125_FG144

RMCF 1/16S 10 5% R
1.5V R98 4.7 ohm
L6 COIL1UH_0805 LQM21FN1R0N
C100 10 nF
C44 4.7uF

Technologic Systems	Date March 15, 2010	
Title: TS-4200 FPGA		
Rev:	Designer	Sheet 3 of 7

3.3V Supply

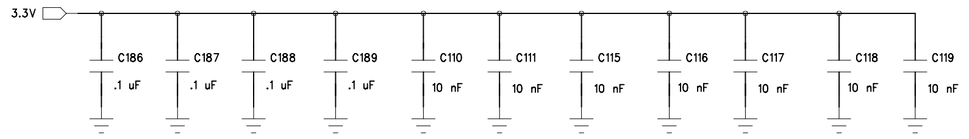


300 mohm max ON resistance
< 100mV drop out @ 250 mA

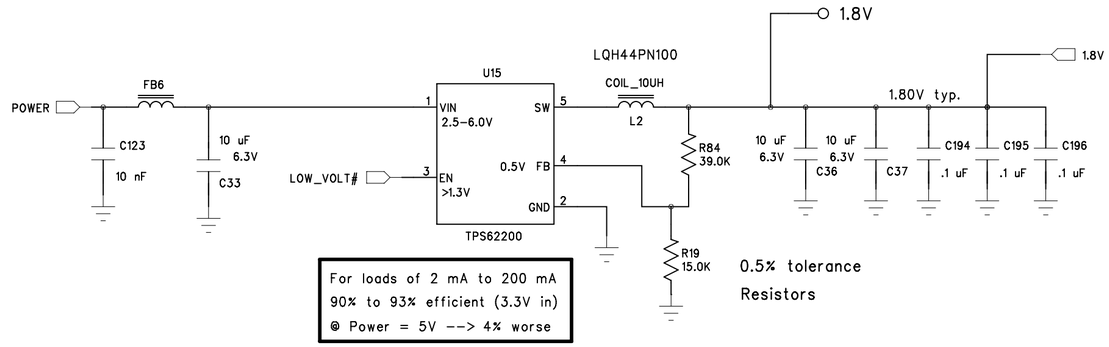
UV lockout is 2.3V

L3 = LQH44PN3R3

Max. current = 1.7 Amps



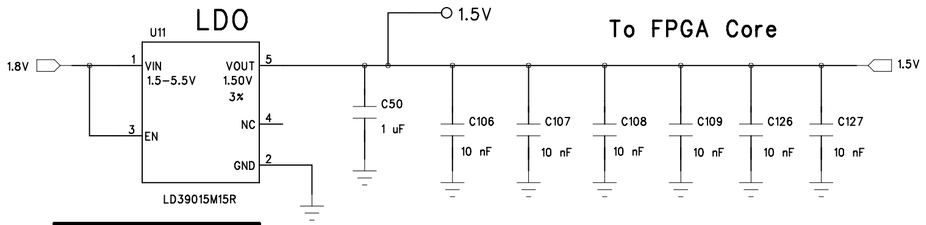
1.8V Supply



For loads of 2 mA to 200 mA
90% to 93% efficient (3.3V in)
@ Power = 5V --> 4% worse

0.5% tolerance
Resistors

1.5V Supply



150 mA max load
100mV drop out
stable with 1 uF ceramic
25 uS Turn-on

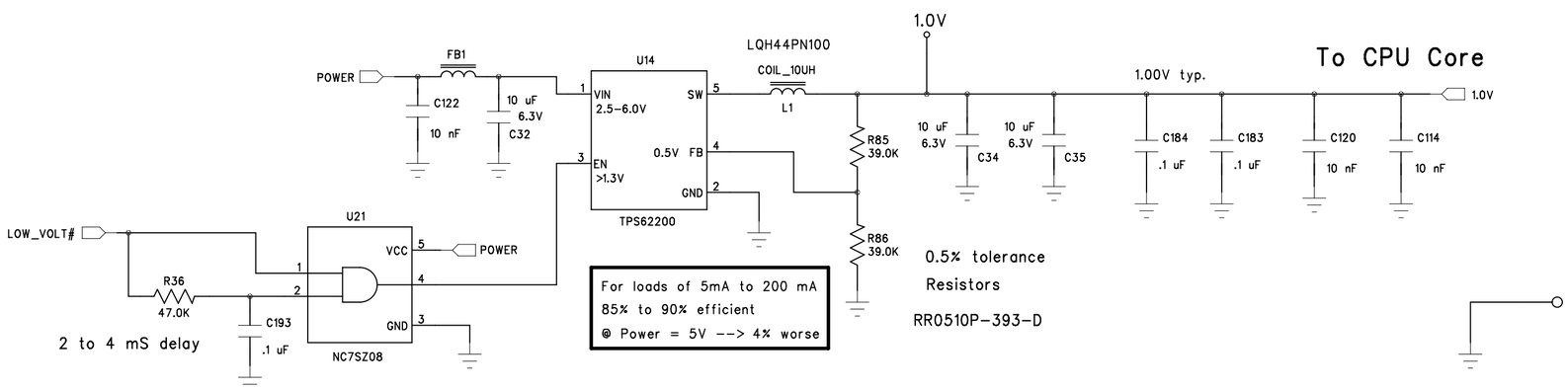
Power Sequence

After power is first applied, or after a "Reboot"
All power rails are off for 200 mS then:

- the 3.3V and 1.8V are enabled
  these will reach 95% in about 800 uS
  (the 1.5V rail will ramp 25 uS delayed)
- Then 2–4 mS later, the 1.0V rail is enabled
  It also requires about 800 uS to ramp

CPU Reset# is asserted before 1.0V rail is enabled

1.0V Supply

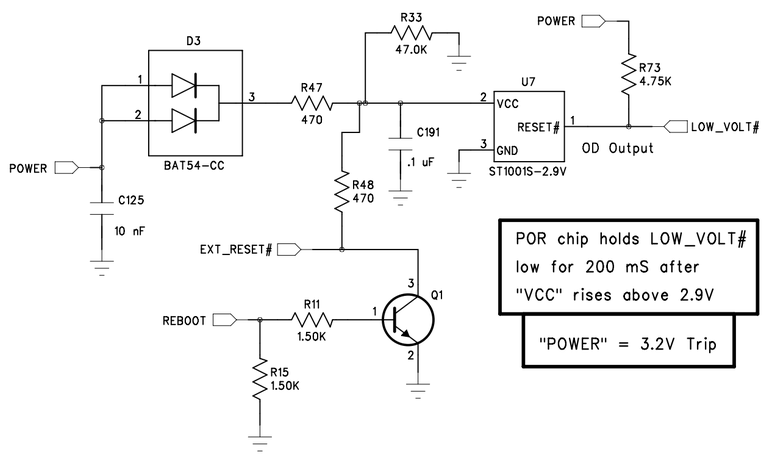


For loads of 5mA to 200 mA
85% to 90% efficient
@ Power = 5V --> 4% worse

0.5% tolerance
Resistors

RR0510P-393-D

POR

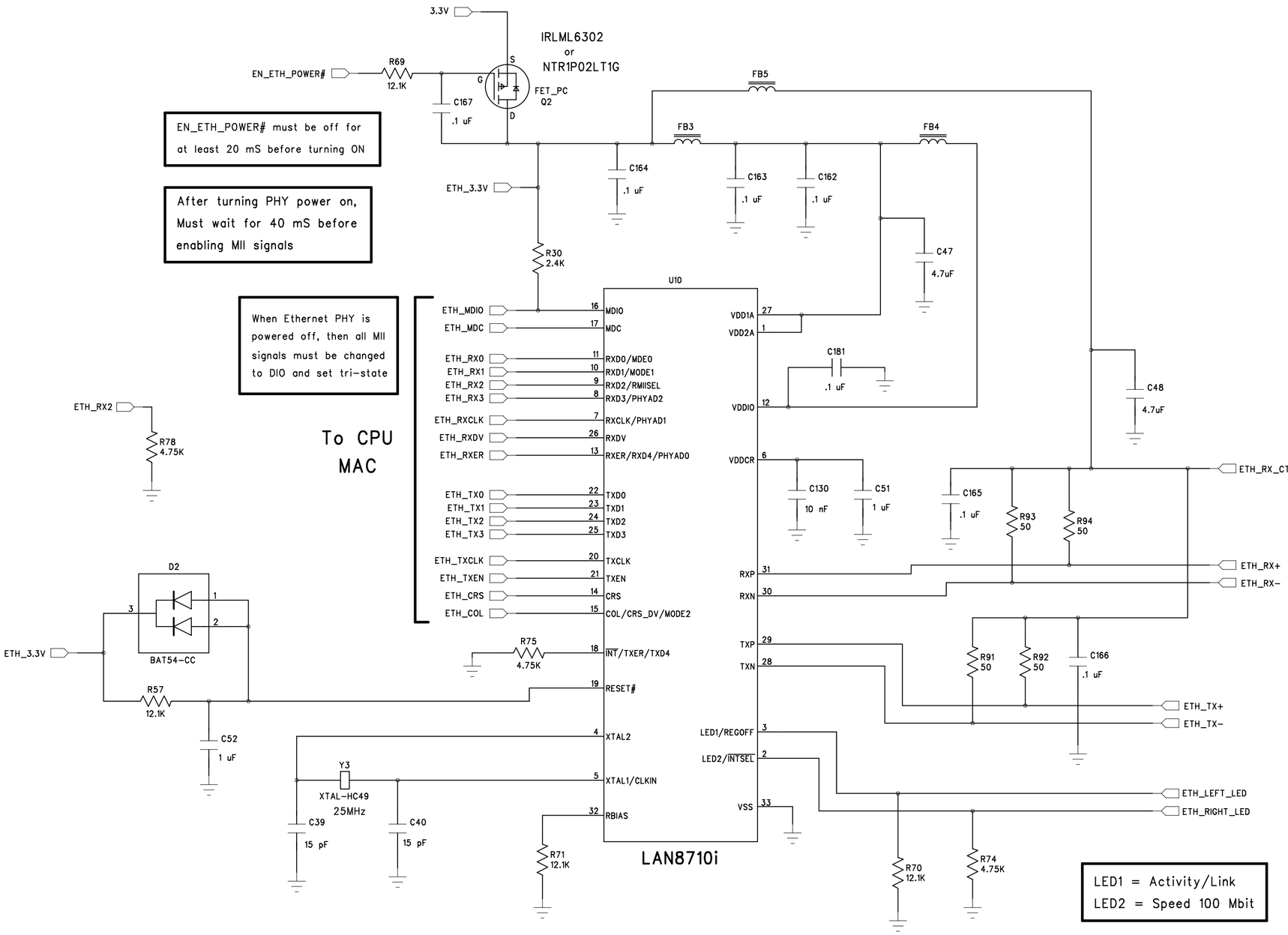


POR chip holds LOW_VOLT# low for 200 mS after "VCC" rises above 2.9V

"POWER" = 3.2V Trip

Technologic Systems	Date March 15, 2010	
Title: TS-4200 Power Supplies and POR		
Rev:	Designer RLM	Sheet 4 of 7

10/100 Ethernet



EN_ETH_POWER# must be off for at least 20 mS before turning ON

After turning PHY power on, Must wait for 40 mS before enabling MII signals

When Ethernet PHY is powered off, then all MII signals must be changed to DIO and set tri-state

LED1 = Activity/Link
LED2 = Speed 100 Mbit

MDIO bus can not be used until 100 uS after Reset# is deasserted

MDCLK max is 2.5 MHz

PHY PU and PD resistors are 67K ohm typical

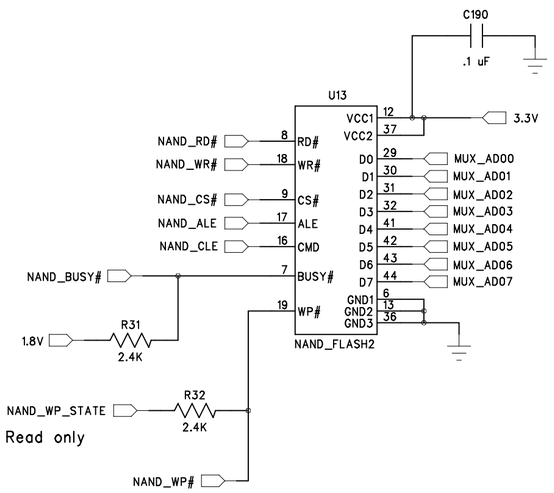
CPU PU resistors are 70K typ. and 40K min.

Beware

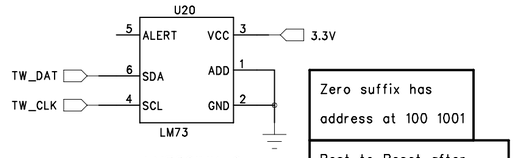
The PHY address is controlled by strapping pins. If CPU has PU; PHY has PD --> indeterminent

Technologic Systems	Date March 15, 2010	
Title: TS-4200 Ethernet PHY		
Rev:	Designer	Sheet 5 of 7

512 MB or 2 GB NAND Flash



Temp Sensor

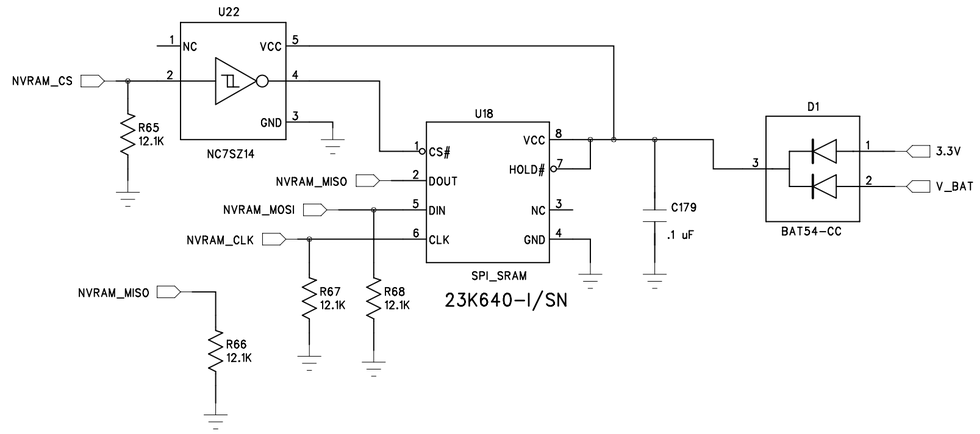


Zero suffix has address at 100 1001

Best to Reset after all power cycles

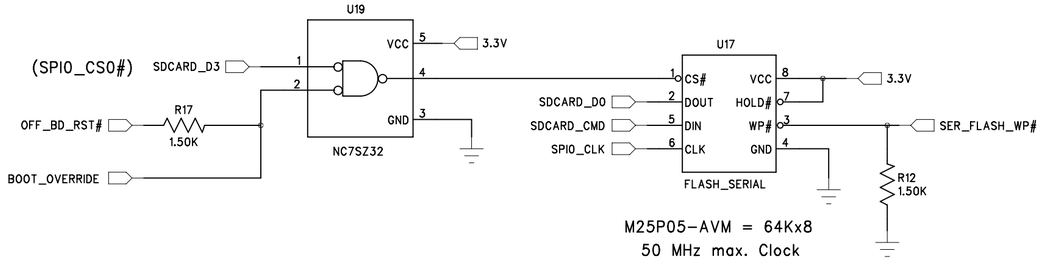
Set PD bit, Wait 50 mS Then clear PD bit

8K Byte NVRAM

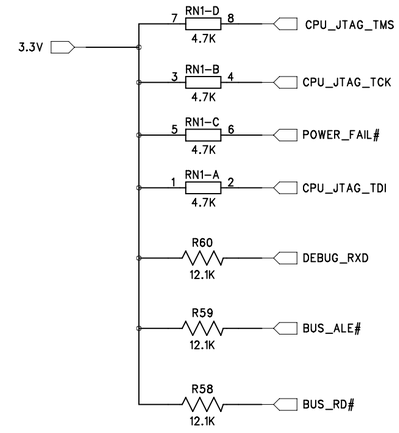


64KB Serial Boot Flash

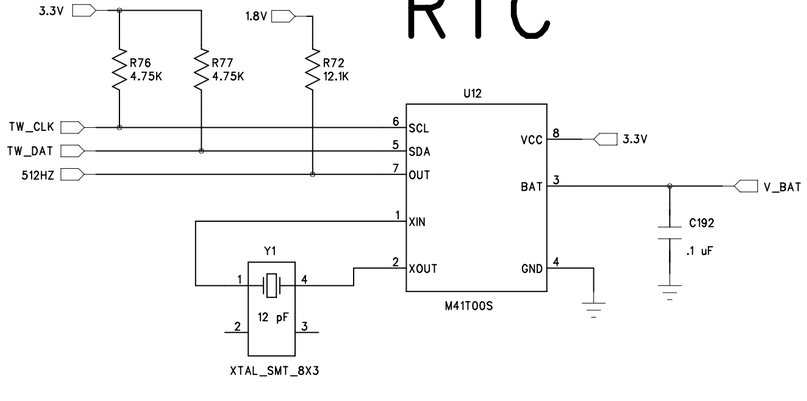
Boot using SPI0 Port



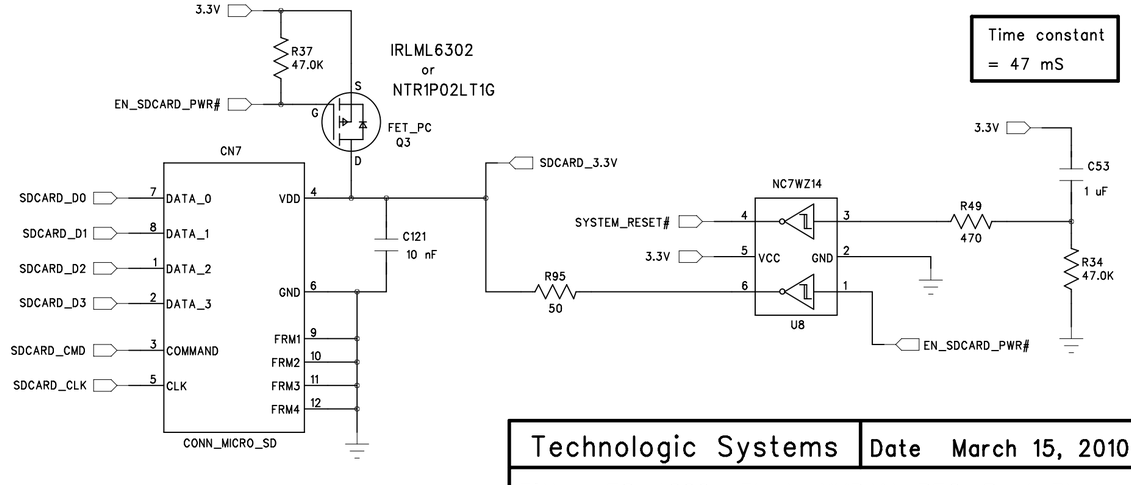
M25P05-AVM = 64Kx8
50 MHz max. Clock



RTC



Micro SD Card Socket



Time constant = 47 mS

Technologic Systems	Date March 15, 2010	
Title: TS-4200 Flash, NVRAM, RTC, Boot Flash		
Rev:	Designer	Sheet 6 of 7

Two 100-pin Off-board Connectors

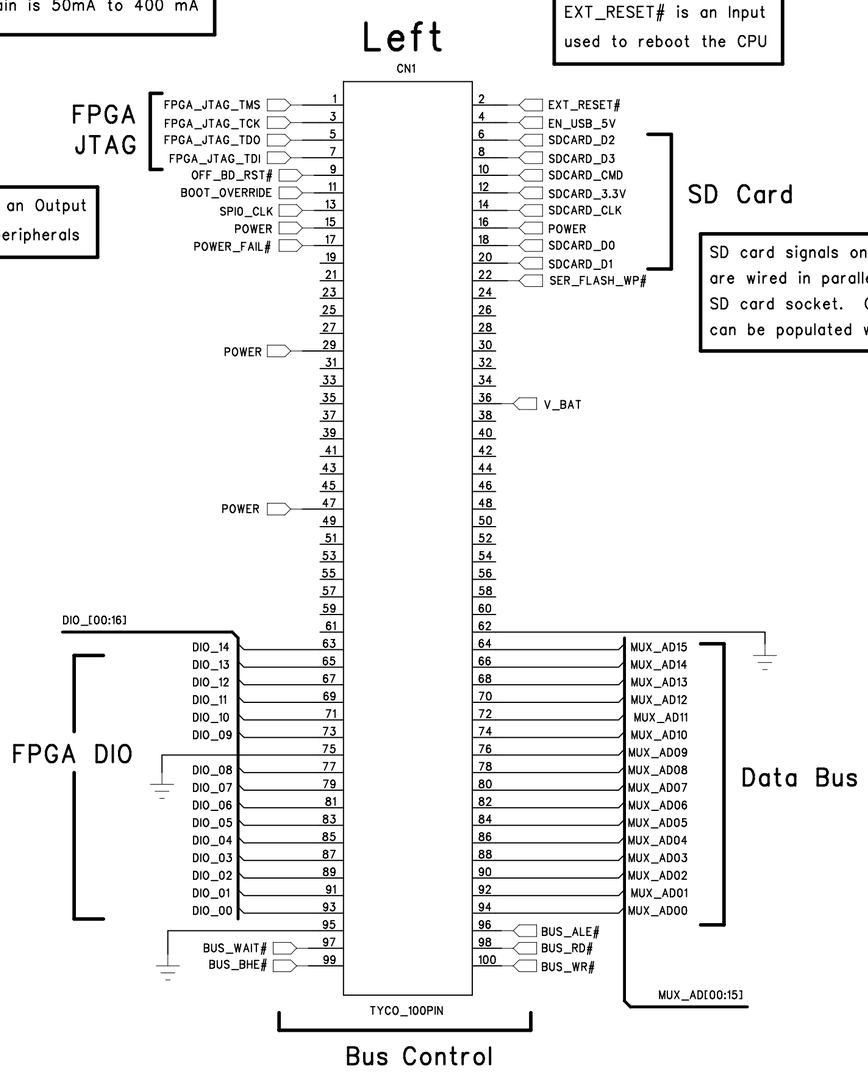
"POWER" pins supply all power to the module
Apply 3.6V to 5.5V to these pins

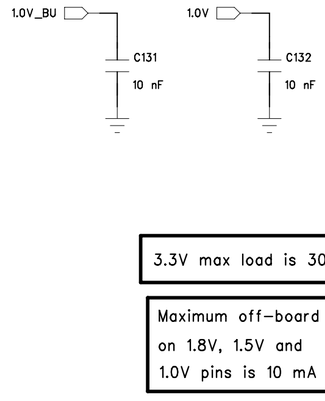
Current drain is 50mA to 400 mA

OFF_BD_RESET# is an Output
used to reset all peripherals

EXT_RESET# is an Input
used to reboot the CPU

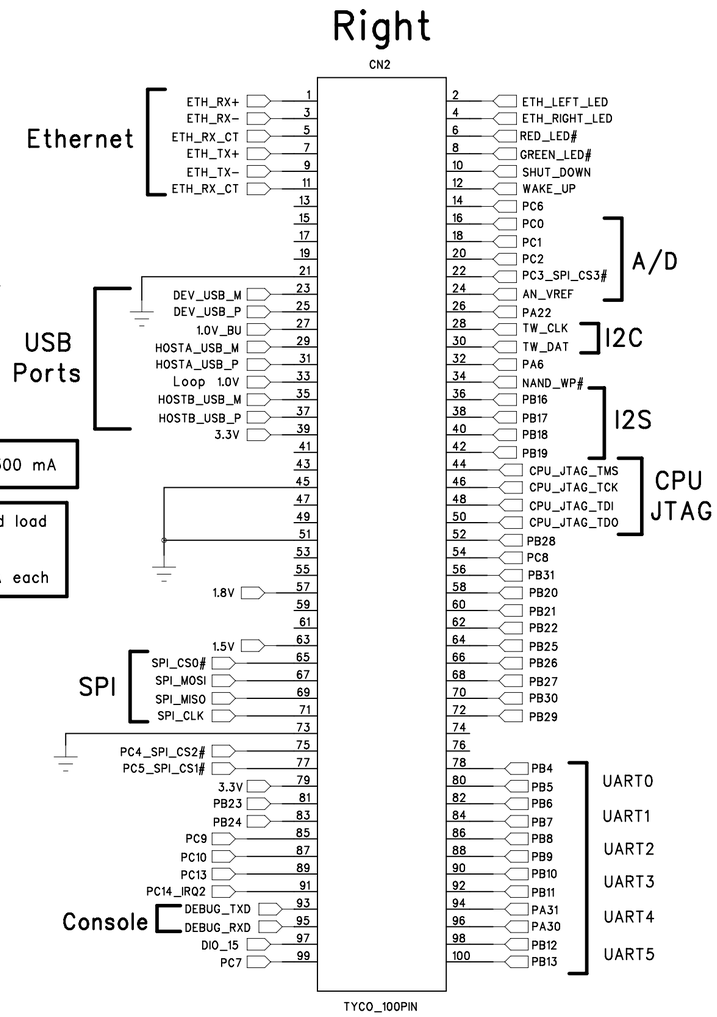
SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card





3.3V max load is 300 mA

Maximum off-board load
on 1.8V, 1.5V and
1.0V pins is 10 mA each



Max. load on JTAG_Vcc
(CN2-79) is 20 mA

These DIO have 1.8V levels

PC4, PC5, PC6
PC7, PC8, PC9
PC10, PC13, PC14

Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1
BUS_RD# = MODE2

MODE1 and MODE2 states
are latched prior to
OFF_BD_RESET# deasserted

MODE1 and MODE2
have PU resistors

Use 1.5K ohm resistor
to "OFF_BD_RESET#"
to set Mode pins "low"

Devices connected to this bus must never
drive it when BUS_RD# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

If Bus is not needed, the following
can be changed to DIO:

- Bus Control signals
- MUX_AD08 thru 15

DIO_00 can be BUS_IRQ
DIO_01 can be BUS_DIR
DIO_02 can be BUS_CS2#
DIO_03 can be BUS_CS3#
DIO_04 can be BUS_CS4#
DIO_05 can be BUS_CS5#

Technologic Systems	Date March 15, 2010	
Title: TS-4200 Off-board Connectors		
Rev:	Designer	Sheet 7 of 7