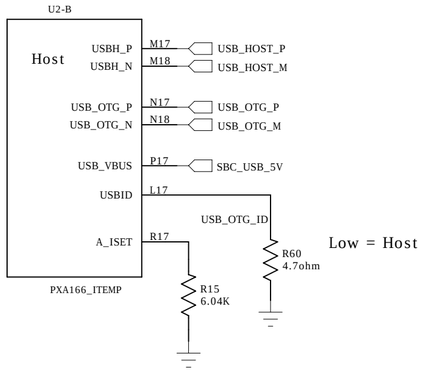
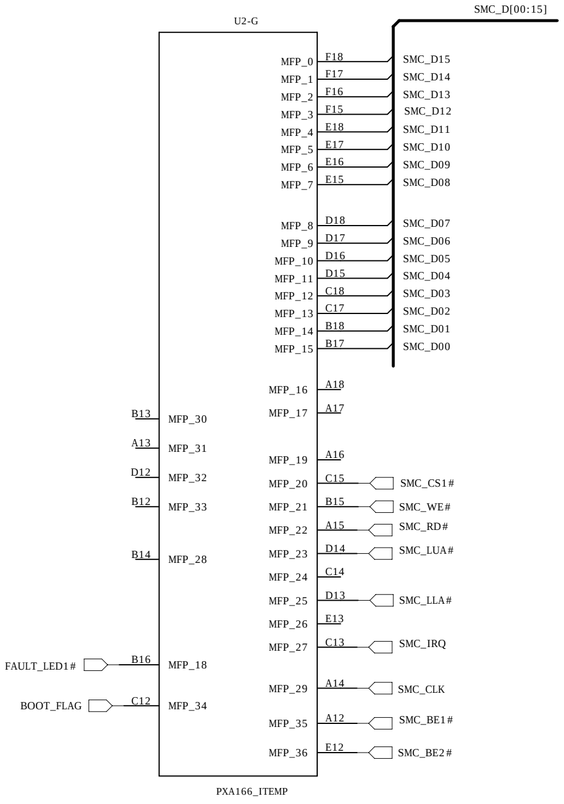
PXA166 800 MHz - PXA168 1066 MHz

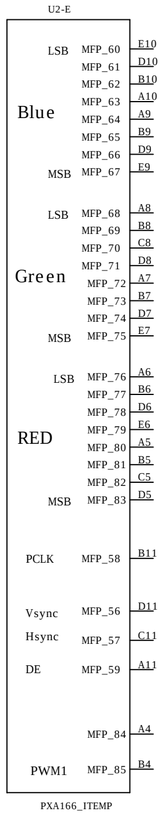
USB Ports



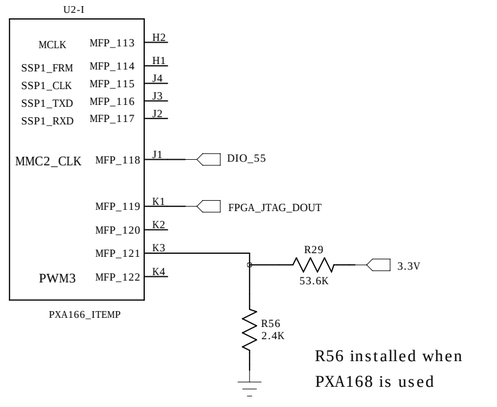
SMC Bus



LCD

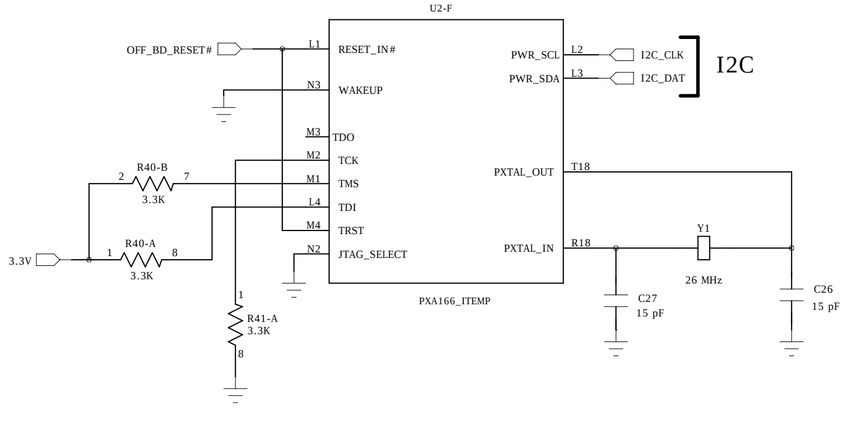


I2S

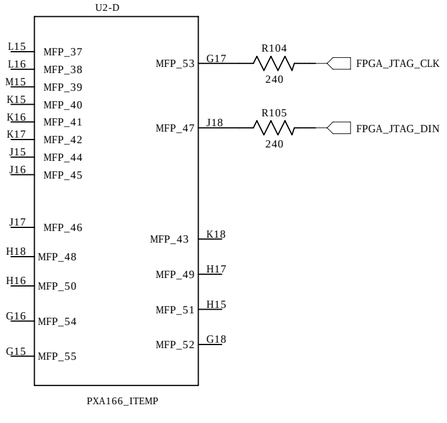


R56 installed when PXA168 is used

Control



Camera



Technologic Systems	Date April 2, 2013	
Title: TS-7700 Marvell PXA166 or PXA168		
Rev: A	Designer	Sheet 1 of 9

DDR3 x8 RAM

2 Gbit RAM chips

512 MB RAM Total

CPU

U2-A

RAM_A[00:14]

RAM_A00 R10 MA_0
RAM_A01 U10 MA_1
RAM_A02 V10 MA_2
RAM_A03 R11 MA_3
RAM_A04 U11 MA_4
RAM_A05 V11 MA_5
RAM_A06 V12 MA_6
RAM_A07 U12 MA_7
RAM_A08 T12 MA_8
RAM_A09 R12 MA_9
RAM_A10 V13 MA_10
RAM_A11 U13 MA_11
RAM_A12 R13 MA_12
RAM_A13 P13 MA_13
RAM_A14 R14 MA_14

RAM_BA0 T9 SDBA0
RAM_BA1 R9 SDBA1
RAM_BA2 P10 SDBA2

RAM_RAS# V8 SDRAS#
RAM_CAS# V9 SDCAS#
RAM_WE# U9 SDWE#
RAM_CS0# R8 SDCS0#
RAM_CKE0 R7 SDCKE0

RAM_CLK V6 SDCLK0
RAM_CLK# V7 SDCLK0#

RAM_LDM P1 DQM0
RAM_UDM V2 DQM1

RAM_LDQS T1 DQS0
RAM_LDQS# R1 DSQ0#
RAM_UDQS V5 DSQS1
RAM_UDQS# V4 DQS1#

RAM_ODT0 U8 ODT

RAM_D[00:15]

MDQ_0 P2 RAM_D04
MDQ_1 P3 RAM_D02
MDQ_2 P4 RAM_D00
MDQ_3 R3 RAM_D05
MDQ_4 T3 RAM_D06
MDQ_5 U1 RAM_D01
MDQ_6 U2 RAM_D03
MDQ_7 V1 RAM_D07

MDQ_8 V3 RAM_D12
MDQ_9 U4 RAM_D09
MDQ_10 R5 RAM_D10
MDQ_11 T5 RAM_D14
MDQ_12 P6 RAM_D08
MDQ_13 R6 RAM_D13
MDQ_14 T6 RAM_D11
MDQ_15 U7 RAM_D15

SDCKE1 N9
SDCS1# N10
ODT1 U14
Output DDRESET# V14 RAM_RST#
CALPAD N4
VREF N1
SEC_CS_EN N5

R108 240
R66 4.75K
R75 4.75K
C188 .1 uF
DDR_1.5V
3.3V
R68 4.75K

PXA166_ITEMP

RAM_UDQS#
RAM_LDQS#
R82 1.0K
R83 1.0K
DDR_1.5V

RAM_UDQS
RAM_LDQS
R84 1.0K
R85 1.0K

RAM_CKE0
R67 4.75K

U17 256MB

RAM_A[00:14]

RAM_A00 K3 A0
RAM_A01 L7 A1
RAM_A02 L3 A2
RAM_A03 K2 A3
RAM_A04 L8 A4
RAM_A05 L2 A5
RAM_A06 M8 A6
RAM_A07 M2 A7
RAM_A08 N8 A8
RAM_A09 M3 A9
RAM_A10 H7 A10
RAM_A11 M7 A11
RAM_A12 K7 A12
RAM_A13 N3 A13
RAM_A14 N7 A14

A3 NC
F1 NC
F9 NC
H1 NC
H9 NC
J7 NC
A7 NU

RAM_RST# N2 RESET#

RAM_BA0 J2 BA0
RAM_BA1 K8 BA1
RAM_BA2 J3 BA2

RAM_CLK F7 CK
RAM_CLK# G7 CK#
RAM_CKE0 G9 CKE
RAM_CS0# H2 CS#

RAM_RAS# F3 RAS#
RAM_CAS# G3 CAS#
RAM_WE# H3 WE#

RAM_ODT0 G1 ODT

RAM_VREF E1 VREF
J8 VREF

C194 .1 uF
C195 .1 uF

VSS0 A1
VSS1 A8
VSS2 B1
VSS3 D8
VSS4 F2
VSS5 F8
VSS6 J1
VSS7 J9
VSS8 L1
VSS9 L9
VSS10 N1
VSS11 N9

VDD0 A2
VDD1 A9
VDD2 D7
VDD3 G2
VDD4 G8
VDD5 K1
VDD6 K9
VDD7 M1
VDD8 M9

VDDQ0 B9
VDDQ1 C1
VDDQ2 E2
VDDQ3 E9

DDR_1.5V

RAM_D[00:15]

DQ0 B3 RAM_D00
DQ1 C7 RAM_D01
DQ2 C2 RAM_D02
DQ3 C8 RAM_D03
DQ4 E3 RAM_D04
DQ5 E8 RAM_D05
DQ6 D2 RAM_D06
DQ7 E7 RAM_D07

DQS C3 RAM_LDQS
DQS# D3 RAM_LDQS#
DM B7 RAM_LDM
ZQ H8

R102 240

VSSQ0 B2
VSSQ1 B8
VSSQ2 C9
VSSQ3 D1
VSSQ4 D9

RAM_DDR3_X8_78BALL

U18 256MB

RAM_A[00:14]

RAM_A00 K3 A0
RAM_A01 L7 A1
RAM_A02 L3 A2
RAM_A03 K2 A3
RAM_A04 L8 A4
RAM_A05 L2 A5
RAM_A06 M8 A6
RAM_A07 M2 A7
RAM_A08 N8 A8
RAM_A09 M3 A9
RAM_A10 H7 A10
RAM_A11 M7 A11
RAM_A12 K7 A12
RAM_A13 N3 A13
RAM_A14 N7 A14

A3 NC
F1 NC
F9 NC
H1 NC
H9 NC
J7 NC
A7 NU

RAM_RST# N2 RESET#

RAM_BA0 J2 BA0
RAM_BA1 K8 BA1
RAM_BA2 J3 BA2

RAM_CLK F7 CK
RAM_CLK# G7 CK#
RAM_CKE0 G9 CKE
RAM_CS0# H2 CS#

RAM_RAS# F3 RAS#
RAM_CAS# G3 CAS#
RAM_WE# H3 WE#

RAM_ODT0 G1 ODT

RAM_VREF E1 VREF
J8 VREF

C196 .1 uF
C197 .1 uF

VSS0 A1
VSS1 A8
VSS2 B1
VSS3 D8
VSS4 F2
VSS5 F8
VSS6 J1
VSS7 J9
VSS8 L1
VSS9 L9
VSS10 N1
VSS11 N9

VDD0 A2
VDD1 A9
VDD2 D7
VDD3 G2
VDD4 G8
VDD5 K1
VDD6 K9
VDD7 M1
VDD8 M9

VDDQ0 B9
VDDQ1 C1
VDDQ2 E2
VDDQ3 E9

DDR_1.5V

RAM_D[00:15]

DQ0 B3 RAM_D08
DQ1 C7 RAM_D09
DQ2 C2 RAM_D10
DQ3 C8 RAM_D11
DQ4 E3 RAM_D12
DQ5 E8 RAM_D13
DQ6 D2 RAM_D14
DQ7 E7 RAM_D15

DQS C3 RAM_UDQS
DQS# D3 RAM_UDQS#
DM B7 RAM_UDM
ZQ H8

R103 240

VSSQ0 B2
VSSQ1 B8
VSSQ2 C9
VSSQ3 D1
VSSQ4 D9

RAM_DDR3_X8_78BALL

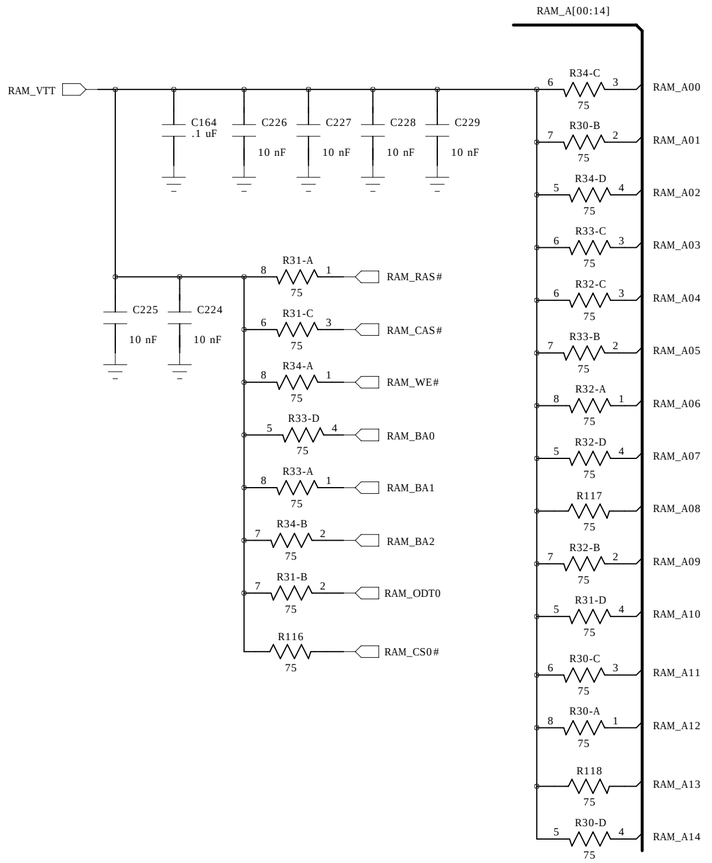
C187 .1 uF
C172 .1 uF
C173 .1 uF
C174 .1 uF
C175 .1 uF
C176 .1 uF
C177 .1 uF
C178 .1 uF
DDR_1.5V

C186 .1 uF
C179 .1 uF
C180 .1 uF
C181 .1 uF
C182 .1 uF
C183 .1 uF
C184 .1 uF
C185 .1 uF
DDR_1.5V

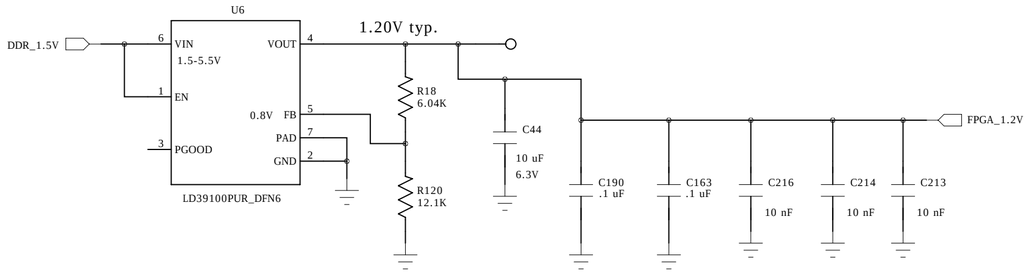
C148 .1 uF
C166 .1 uF
DDR_1.5V

Technologic Systems		Date April 2, 2013
Title: TS-7700 DDR3 RAM		
Rev: A	Designer	Sheet 2 of 9

Termination Resistors

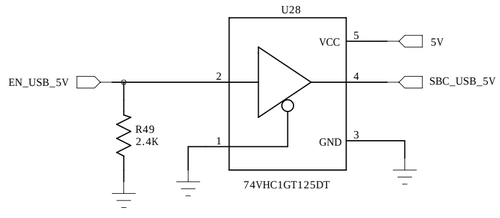


FPGA 1.2V Reg.



3.3V --> 5V

Level Shifter



Technologic Systems		Date April 2, 2013
Title: TS-7700 DDR3 RAM		
Rev: A	Designer	Sheet 3 of 9

10/100 Ethernet

CPU

U2-C

MDIO MFP_101 D1
MDC MFP_100 F4
RXD0 MFP_99 E3
RXD1 MFP_98 D2
RXD2 MFP_97 C1
RXD3 MFP_96 E4
RX_CK MFP_94 D3
RX_DV MFP_103 F3
RX_ER MFP_95 C2
TXD0 MFP_91 C3
TXD1 MFP_90 B2
TXD2 MFP_89 D4
TXD3 MFP_88 A2
TX_CK MFP_86 A3
TX_EN MFP_87 B3
CRS MFP_92 A1
COL MFP_93 B1
MFP_102 E2 FAULT_LED0#
PWM4 MFP_104 E1
MFP_105 F2
MFP_106 F1

PXA166_ITEMP

R73 4.75K
3.3V
R55 2.4K

U13

MDIO 16
MDC 17
RXD0/MDE0 11
RXD1/MODE1 10
RXD2/RMIISEL 9
RXD3/PHYAD2 8
RXCLK/PHYAD1 7
RXDV 26
RXER/RXD4/PHYAD0 13
TXD0 22
TXD1 23
TXD2 24
TXD3 25
TXCLK 20
TXEN 21
CRS 14
COL/CRS_DV/MODE2 15
INT/TXER/TXD4 18
RESET# 19 VDD_IO max
XTAL2 4
XTAL1/CLKIN 5
RBIAS 32

R69 4.75K
FPGA_RESET#
Y3 25 MHz
C25 15 pF
C24 15 pF
R122 12.1K

LAN8710i

FB5 220 ohm
FB6 220 ohm
C147 .1 uF
C193 .1 uF
C51 1 uF 6.3V

VDD_1A 27
VDD_2A 1
C192 .1 uF
VDD_IO 12 3.3V
VDD_CR 6
C221 10 nF
C49 1 uF 6.3V

1.2V Core

LAN8710 can power sequence in any order

Internal 1.2V Reg. can be turned off by having LED1 high

Using Sw. 1.2V Reg. saves 13 mA @ 5V

Total chip power: 160mw --> 100 mw

C52 1 uF 6.3V

C191 .1 uF
R95 51
R98 51

RXP 31 ETH_RX_P
RXN 30 ETH_RX_M
TXP 29
TXN 28
R96 51
R97 51
C116 .1 uF
ETH_TX_P
ETH_TX_M

LED1/REGOFF 3
VDD_2A
LED2/INTSEL 2
VSS 33
R123 12.1K
R17 6.04K

C211 10 nF
R48 1.0M
U9
FPGA_25MHZ 6 1
3.3V 5 VCC GND 2
4 3
74LVC2GU04DCK

10/100 Ethernet

R59 4.7ohm
C198 .1 uF
C115 .1 uF
C222 10 nF

J5

ETH_TX_P 4 RX+
ETH_TX_M 5 RX-
6 RX_CT
3 TX_CT
ETH_RX_P 1 TX+
ETH_RX_M 2 TX-
ALIGN 17
ALIGN 18
POE_RX 7 POE_RX
POE_TX 8 POE_TX
POE_45 9 POE_45
POE_78 10 POE_78

R112 240
R113 240
11 LLED+
12 LLED-
Green
13 RLED+
14 RLED-
Yellow
SHD 15
SHD 16

RJ_POE_4602
EC-MJKF4602-PA08

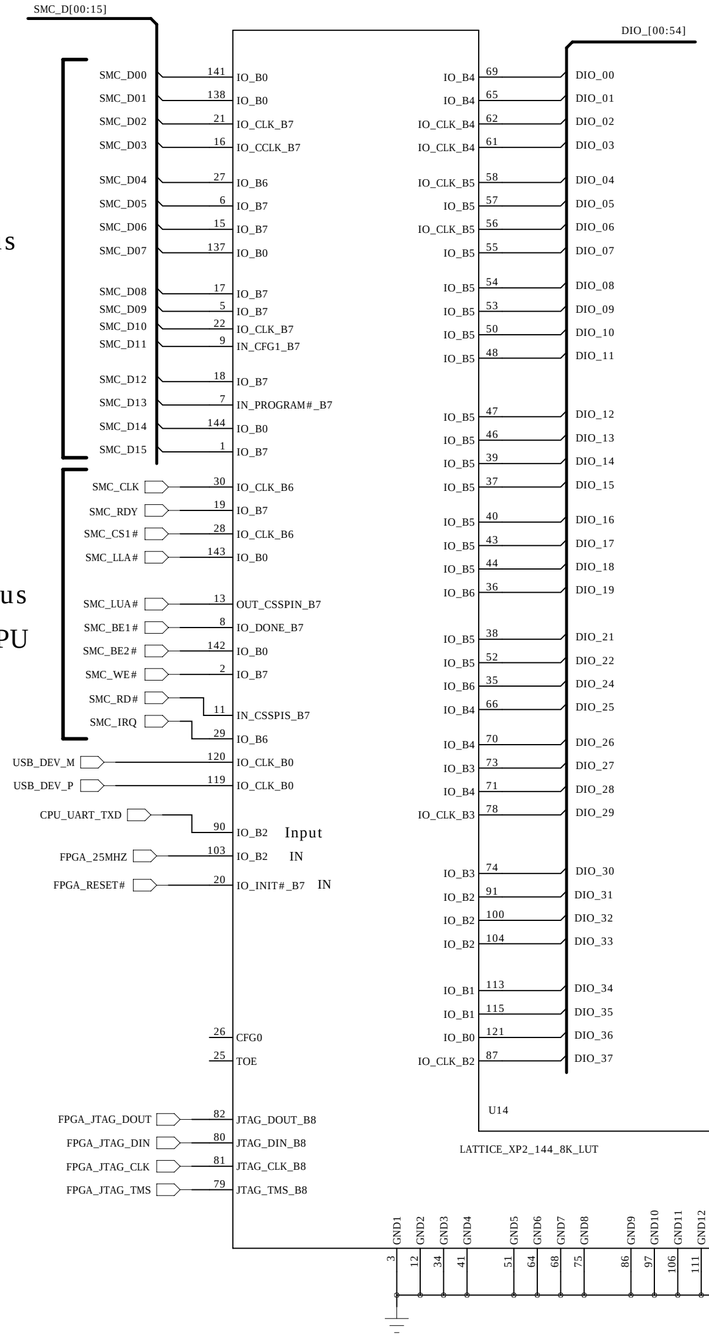
FRAME
FB4 220 ohm

Technologic Systems		Date April 2, 2013
Title: TS-7700 Ethernet PHY		
Rev: A	Designer RLM	Sheet 4 of 9

FPGA with 8000 LUTs

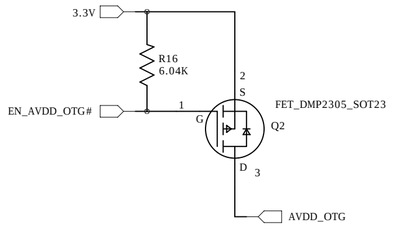
SMC Data Bus

SMC Bus from CPU



SD Cards

CPU USB Power

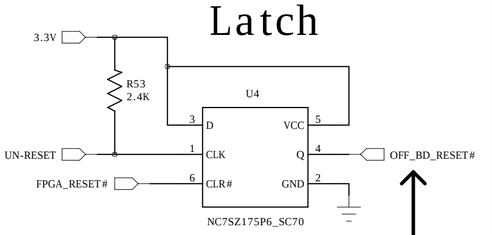


After FPGA_RESET# is deasserted

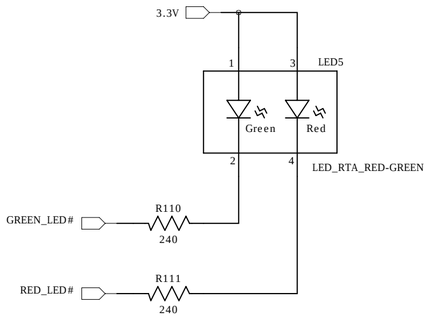
Assert EN_AVDD_OTG#

Then wait another 10-20 mS before "Un-resetting" CPU

Reset Latch



This drives CPU_RESET#



XP2-5 has:
5K or 8K LUTS 2 PLLs
9/12 blocks of 1Kx18 Block RAM
12 18x18 Multipliers

100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Pull-up and pull-down resistors are 6 to 30K ohms

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic

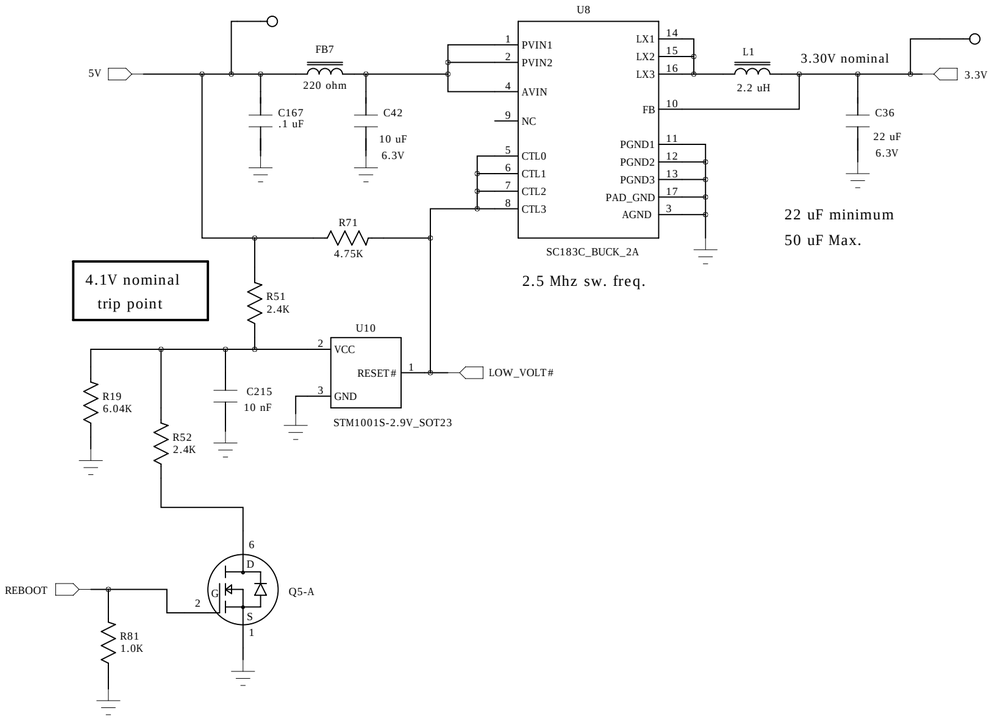
All I/O lines are tri-stated during power cycling

Technologic Systems	Date April 2, 2013	
Title: TS-7700 FPGA		
Rev: A	Designer	Sheet 5 of 9

Power Supplies

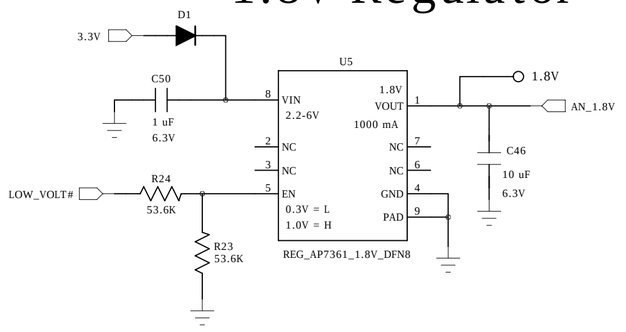
3.3V Power Supply

up to 2000 mA



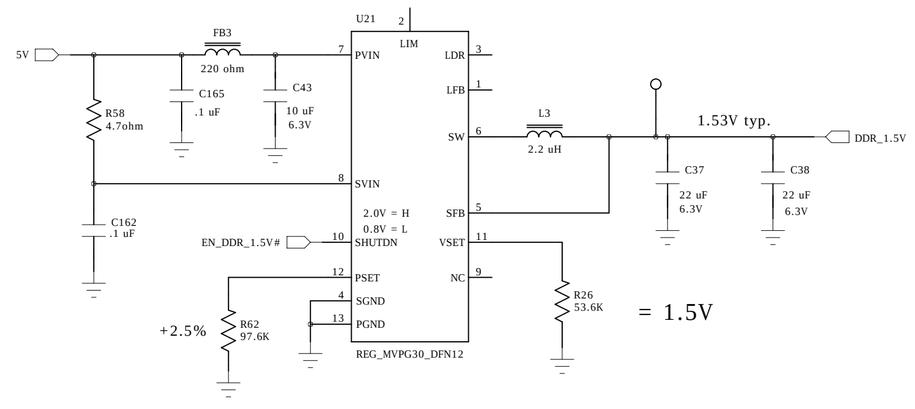
Analog

1.8V Regulator

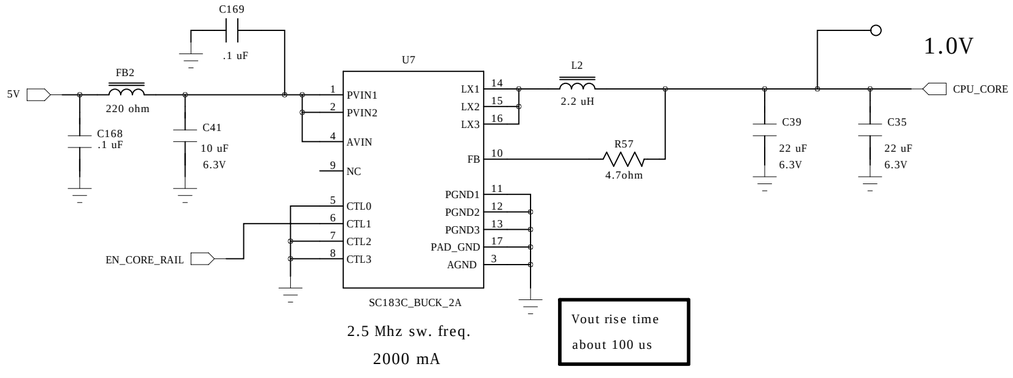


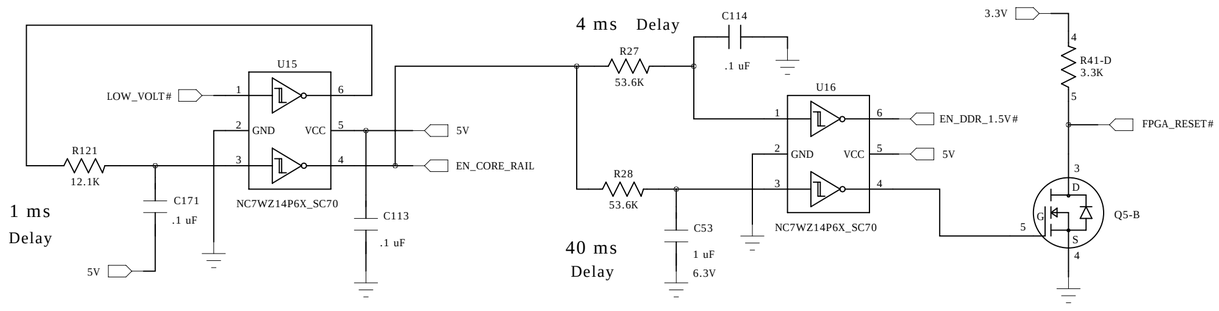
GND

DDR3 1.5V Reg.



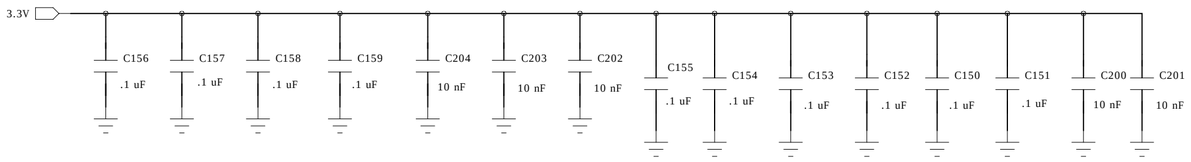
CPU Core Supply

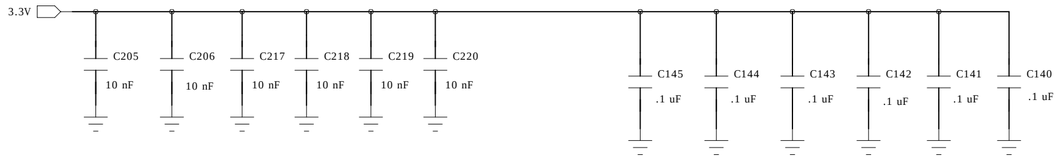


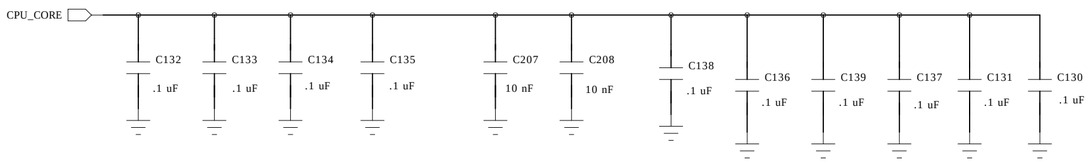


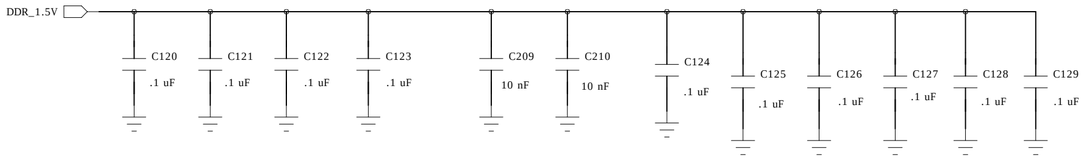
Technologic Systems	Date April 2, 2013	
Title: TS-7700 Power Supplies		
Rev: A	Designer	Sheet 6 of 9

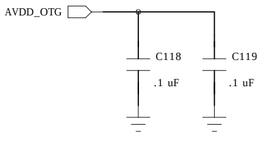
CPU Power

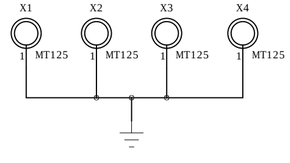






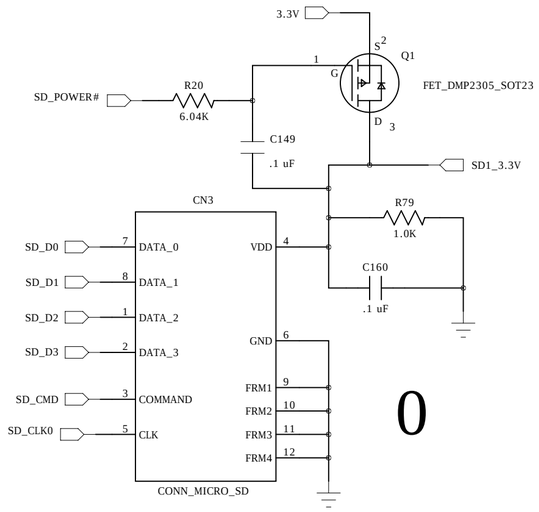




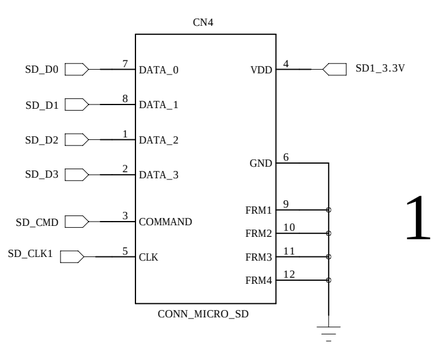


Technologic Systems	Date April 2, 2013	
Title: TS-7700 CPU Power and Bypass caps		
Rev: A	Designer	Sheet 7 of 9

Micro SD Card Sockets

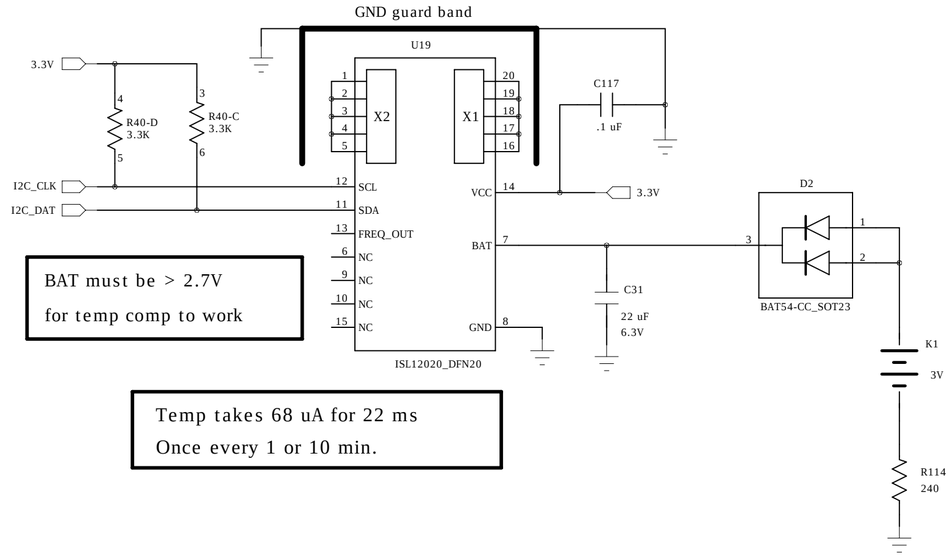


0



1

RTC and Temp. Sensor

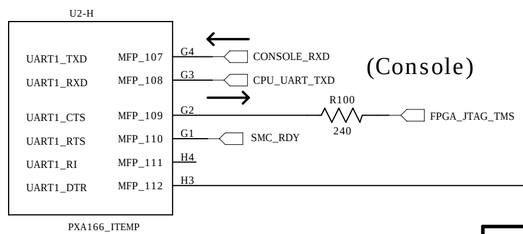


BAT must be > 2.7V
for temp comp to work

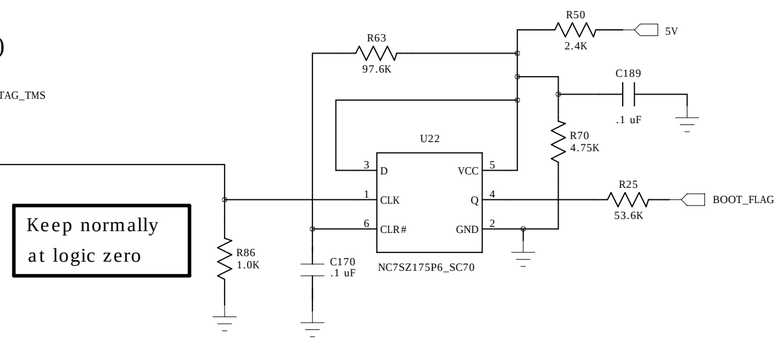
Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

CPU

Debug UART

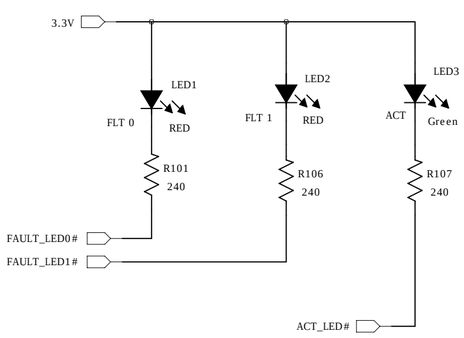


Reboot Flag



Keep normally
at logic zero

SD Card LEDs



Technologic Systems	Date April 2, 2013	
Title: TS-7700 SD card, RTC, Temp.		
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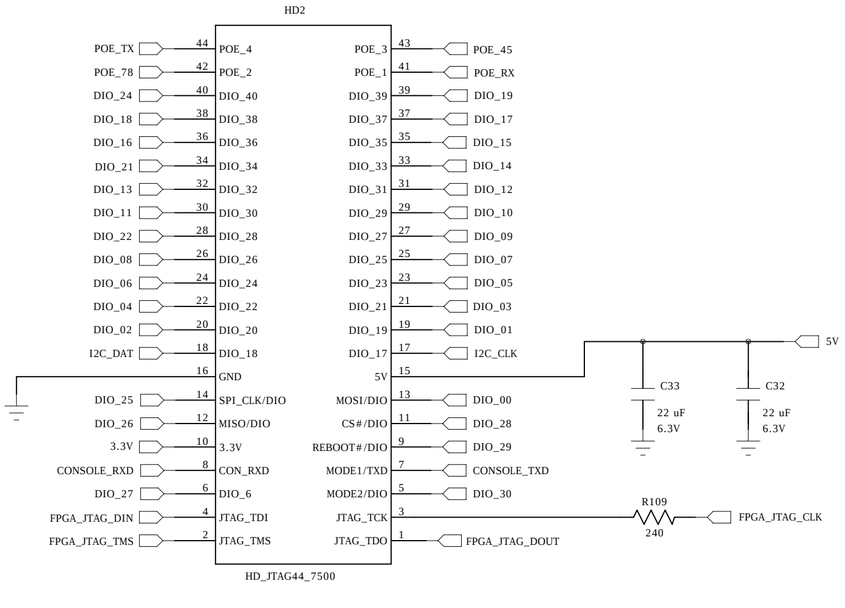
44-Pin DIO Header



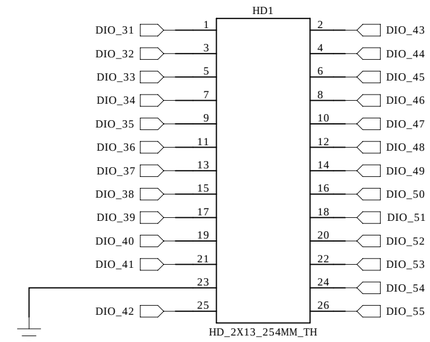
MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Logic "0" on MODE2 signal forces Boot from SD card

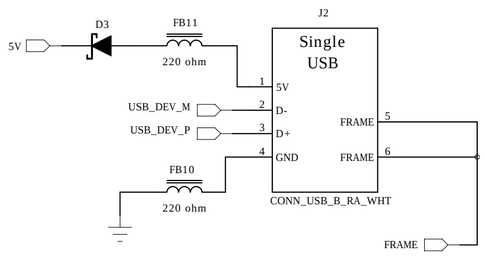
MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Logic "0" on MODE1 forces Console onto the TXD and RXD lines

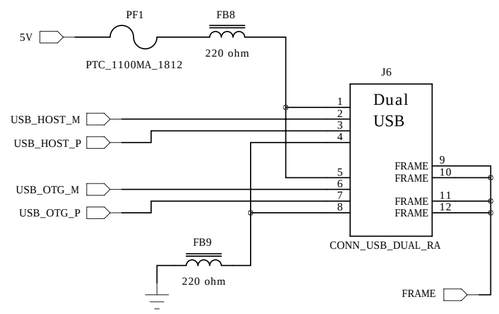
26-Pin DIO Header



USB Device Port



USB Host Ports



Technologic Systems		Date April 2, 2013
Title: TS-7700 DIO Header		
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