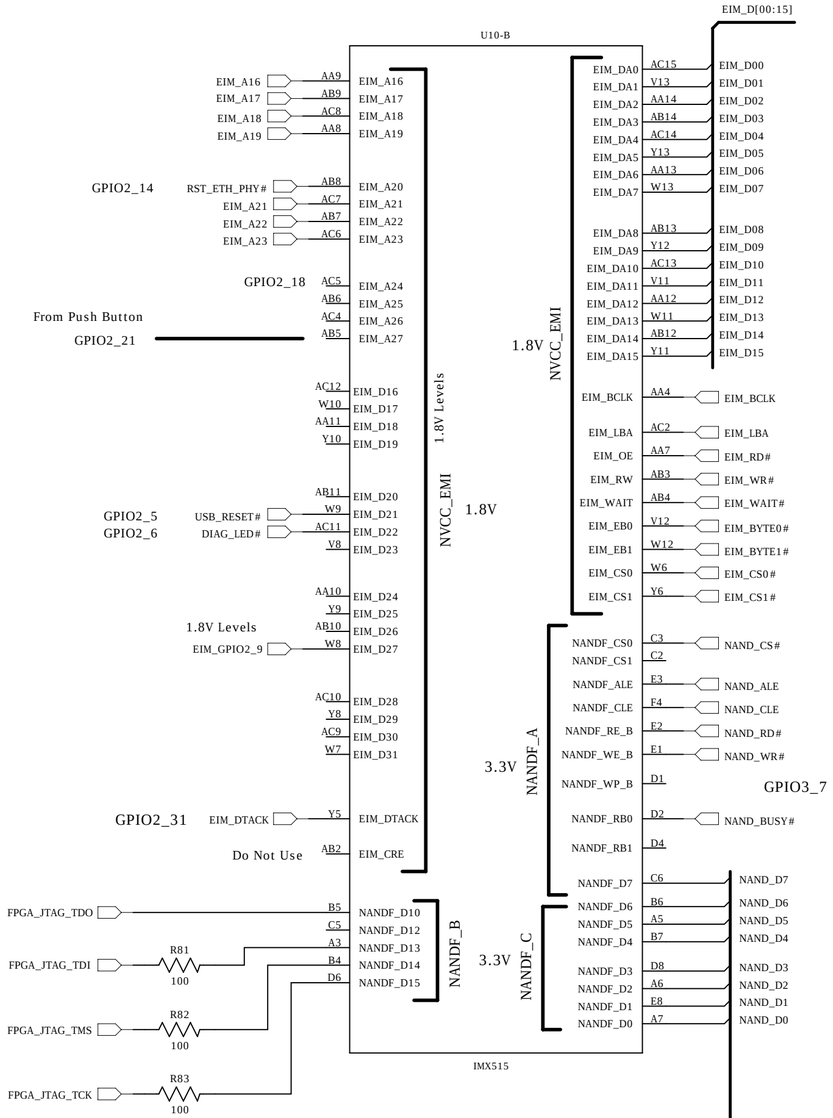
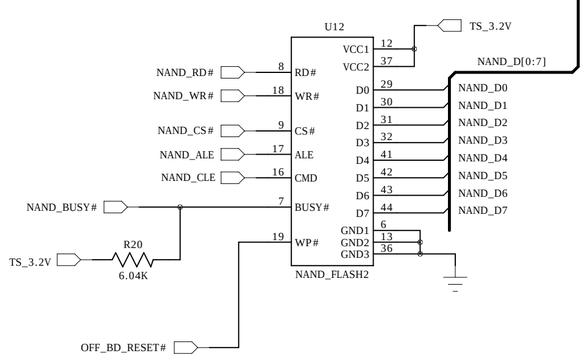
MX515



NAND Flash



MX515

In Ref design
when ID = Low, then
it turns on local 5V
to USB_OTG bus

USB_5V_line should
have 5V on it anytime
OTG device is plugged in
either Device supplies 5V
or else local 5V turned on

I2S
Audio

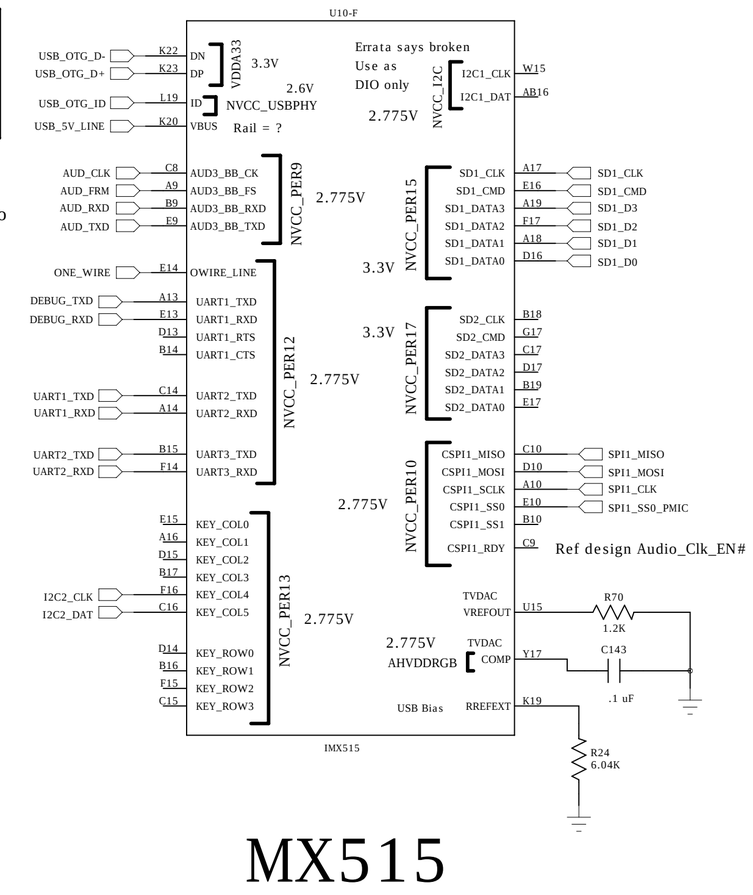
for Code compatibility

RXD low = Babbage-3

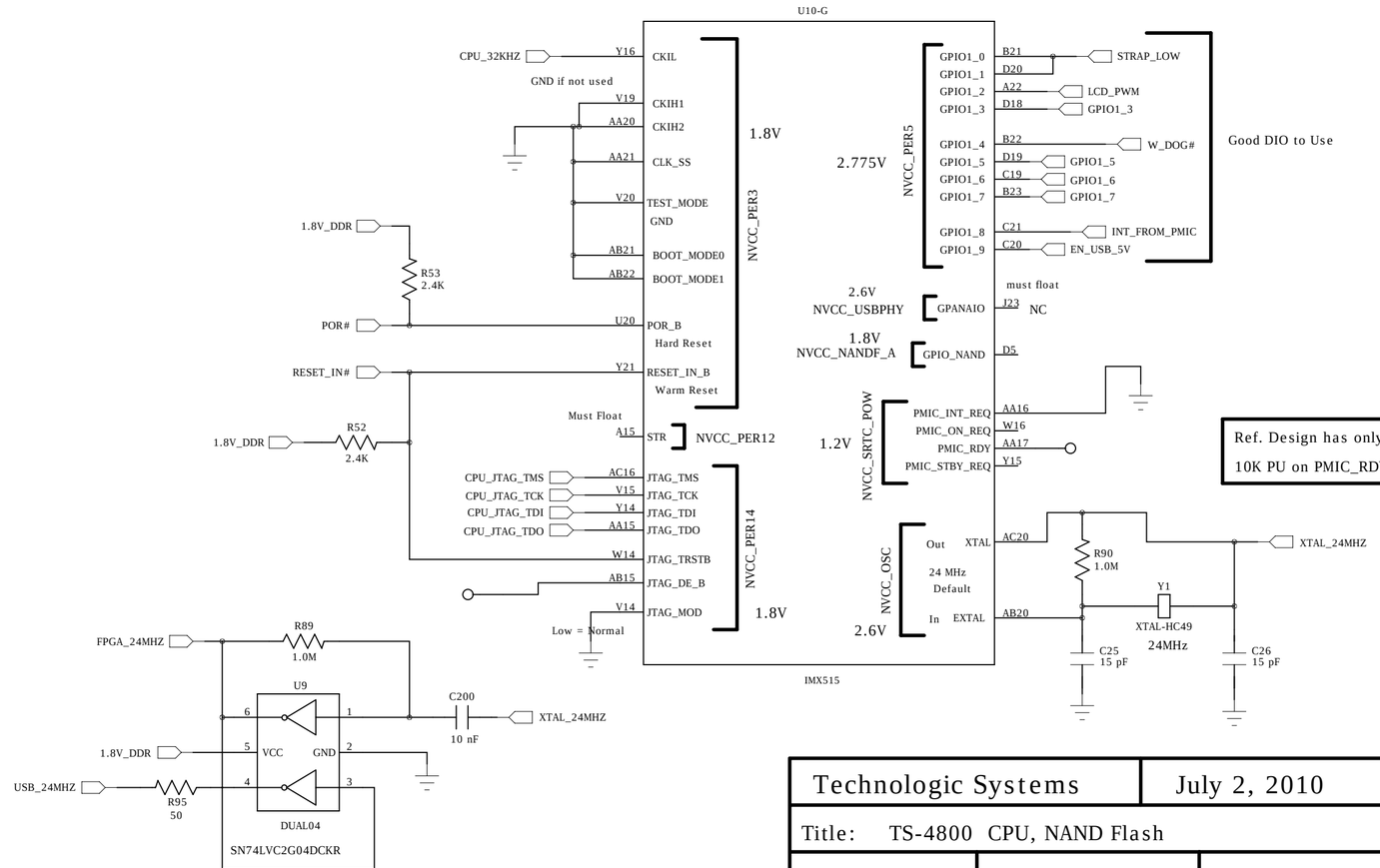
UART3_RXD needs
10K res. to GND

UART3_TXD is input
that turns on system ?

GPIO1_23

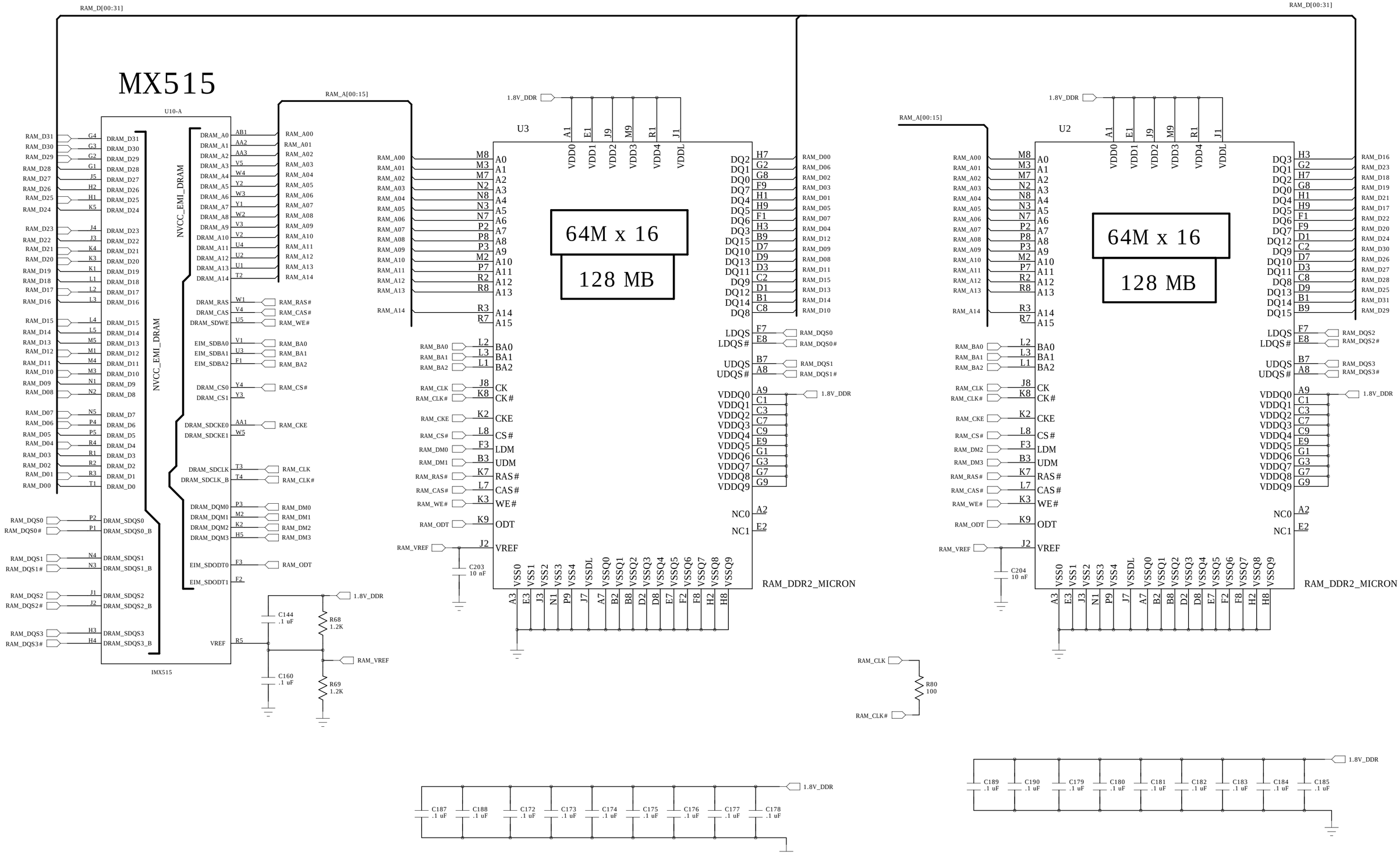


MX515



Technologic Systems		July 2, 2010
Title: TS-4800 CPU, NAND Flash		
Rev:	Designer	Sheet 1 of 9

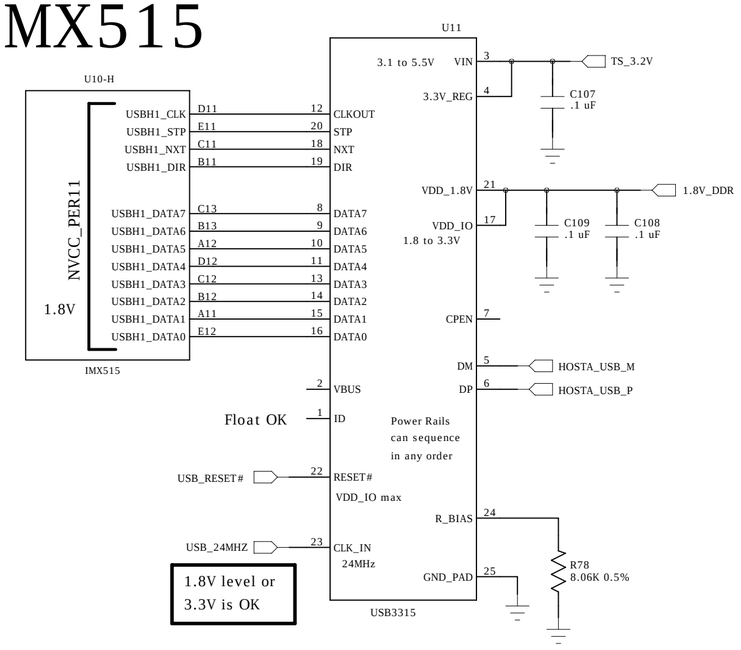
DDR2 SDRAM (256 MByte)



Technologic Systems	July 2, 2010	
Title: TS-4800 DDR2 RAM		
Rev:	Designer	Sheet 2 of 9

USB PHY

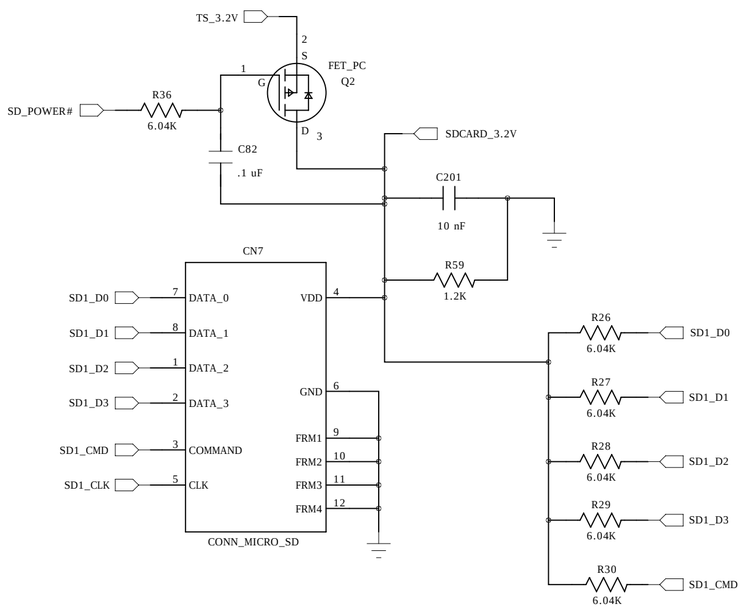
MX515



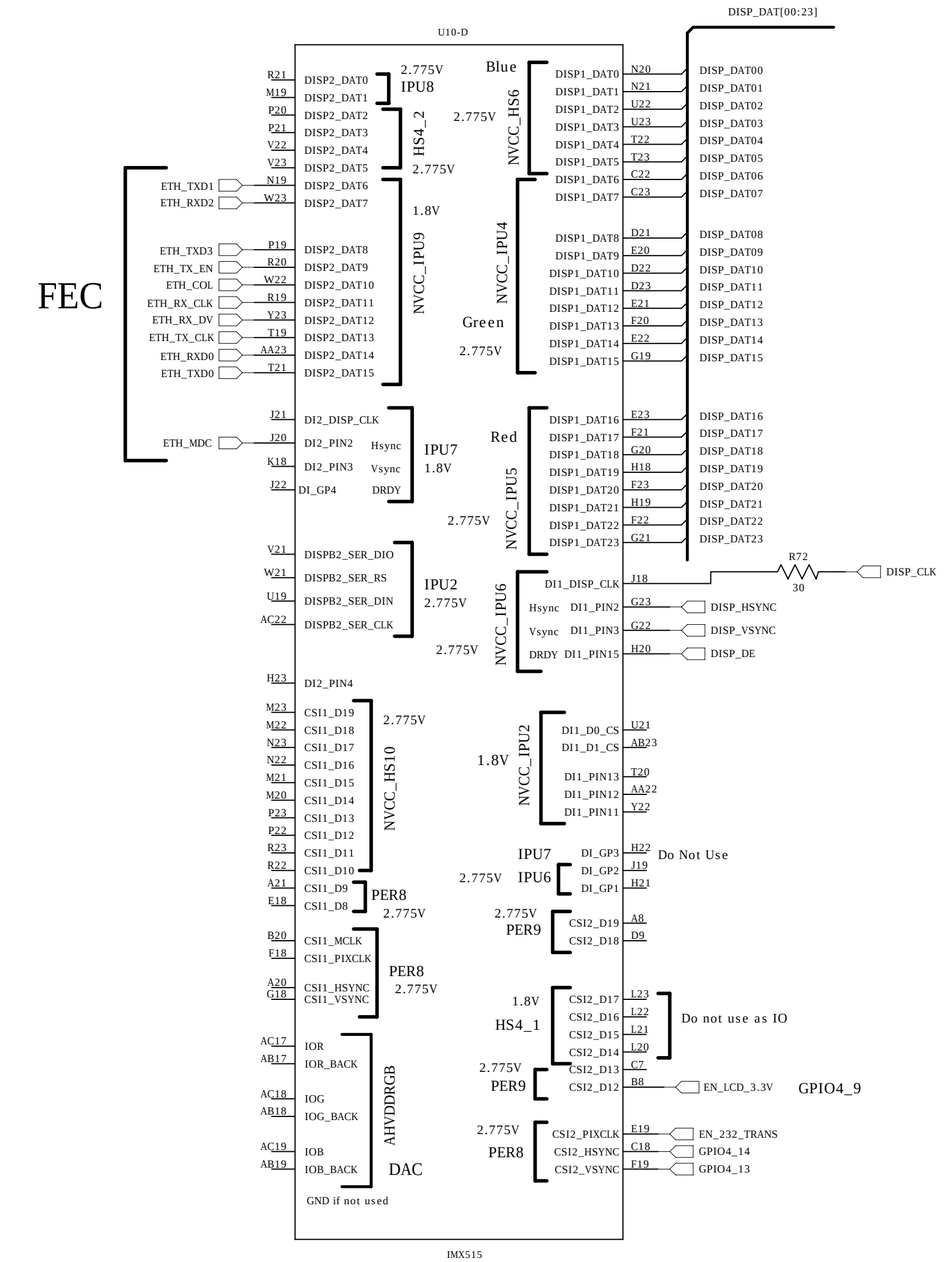
USB3315

HS current drain:	30 mA @ 1.8V
	10 mA @ 3.3V
Reset asserted = 20 uA	
Rated for -40 to +85 degrees	

Micro SD Card Socket



MX515



Technologic Systems	July 2, 2010	
Title: TS-4800 USB PHY, Video, SD card		
Rev:	Designer RLM	Sheet 3 of 9

FPGA with 5000 LUTs

Bank 0 has 20 DIO
Bank 1 has 6 DIO
Bank 2 has 18 DIO
Bank 3 has 4 DIO
Bank 4 has 8 DIO
— 3.3V

Bank 5 has 18 DIO
Bank 6 has 8 DIO
Bank 7 has 18 DIO
— 1.8V

FPGA pins can be swapped
but only pins within
each Power Rail

Set CONFIG_MODE to NONE
This allows all pins to be used

XP2-5 has:

5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

POR# and RESET_IN#
must be Open Drain I/O

Pull-up and pull-down resistors
are 6 to 30K ohms

PMIC_STBY_REQ, PMIC_ON_REQ,
and CPU_32KHZ have 1.2V levels
FPGA must be designed for that

Only FPGA drives CN2

When BP drops below
3.4V - Reset FPGA

RESET_FPGA
is not OD !

LED Outputs
should be OD

Low for 200 mS
3 mS rise time

PROGRAM#, DONE, and INIT# are
dedicated configuration pins when
CFG0 is low. When CFG0 is high
they are "general purpose I/O"
Page 4 of TN1141

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order
but must be monotonic
All I/O lines are tri-stated during power cycling

FPGA 1.2V Reg.

LDO

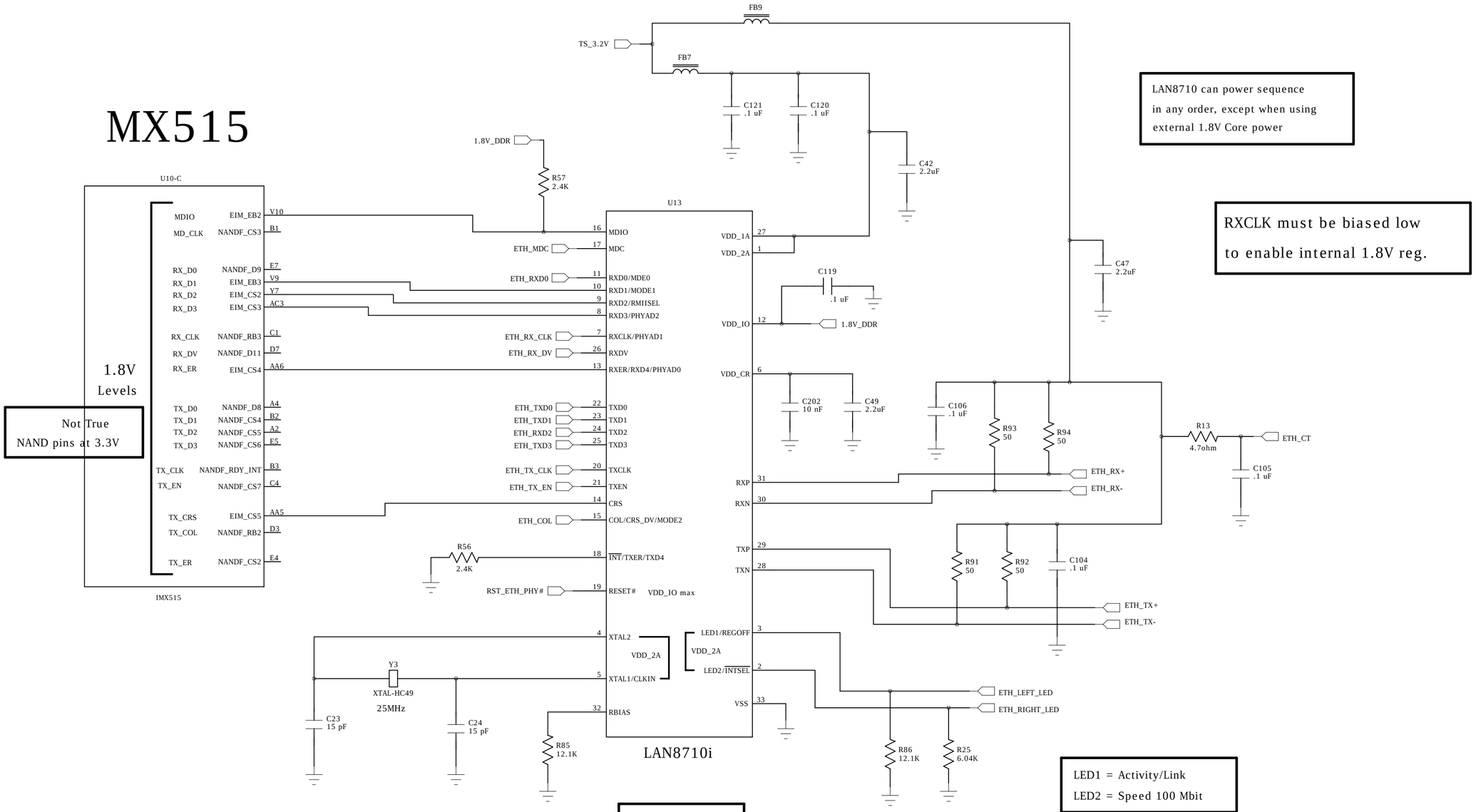
Measured 57 mA with
FPGA 2K LUTs running

300 mA max load
500 mV drop out
25 uS Turn-on

Technologic Systems	July 2, 2010	
Title: TS-4800 FPGA		
Rev:	Designer	Sheet 4 of 9

10/100 Ethernet

MX515



Technologic Systems		July 2, 2010
Title: TS-4800 Ethernet PHY		
Rev:	Designer	Sheet 5 of 9

PMIC

Valid BP is 3.0 to 4.65V
But must rise above 3.2V
to turn on properly

Design Guide says:
BP is 3.7 to 4.2V

U7-A

BP — near pin B11 — C57 2.2uF

BP, BPSNS, BATT, BATTFET (NC), BATTISNS, BATTISNSCC (?)

PWGTDRV1 NC, PWGTDRV2 NC — Outputs for Power Gating

LQH32PN1R5N = 1.5 uH
LQH32PN2R2N = 2.2uH

SW1IN_1, SW1IN_2 — BP — L1 COIL1.5UH — SW1OUT — VDD_GP — 1.05V at reset — ARM Core
1050 mA
SW1FB — SENSE_VDDGP — C35 10 uF 6.3V, C36 10 uF 6.3V, C37 10 uF 6.3V
DVS1 — NC

SW2IN_1, SW2IN_2 — BP — L5 COIL2.2UH — SW2OUT — VCC — 1.225V at Reset — CPU rail
800 mA
SW2FB — SENSE_VCC — C28 10 uF 6.3V
DVS2 — NC

SW3IN_1, SW3IN_2 — BP — L7 COIL2.2UH — SW3OUT — 1.2V_DIG1 — CPU rail
800 mA
SW3FB — C31 10 uF 6.3V

SW4IN_1, SW4IN_2 — BP — L6 COIL2.2UH — SW4OUT — 1.8V_DDR — RAM and CPU Also 1.8V_DIG1
800 mA
SW4FB — C30 10 uF 6.3V

SWBSTIN NC, SWBSTOUT NC, SWBSTFB — ?

VVIDEODRV — NSS12100X — Q1 — R11 1 ohm — BP; R15 0.20; C48 2.2uF; C205 10 nF; C206 10 nF — 2.775V
350 mA
VVIDEO

VINUSB2 — must be BP — BP — 2.4 thru 2.775V
50 mA
VUSB2 — 2.6V — C52 2.2uF

VINAUDIO — BP
150 mA
VAUDIO — NC

VINIOHI — must be BP — BP — C51 2.2uF — 2.775V_BOOT
100 mA
VIOHI

VINPLL — >2.2V — BP — C50 2.2uF — 1.8V_ANA_PLL
50 mA
VPLL

VINDIG — >2.2V — BP
50 mA
VDIG — NC

VINCAMDRV — NC
65 mA or 250 mA
VCAM — 2.50 to 3.00V

VSDDRV — NC
250 mA
VSD — NC

VGEN1DRV — NC
200 mA
VGEN1 — NC

VGEN2DRV — NC
350 mA
VGEN2 — NC

VINGEN3DRV — NC if not used
50 mA or 200 mA
VGEN3 — NC if not used

REFCORE — 1.2V — C162 .1 uF
VCORE — 2.775V — C53 2.2uF; R12 100K

only 2 places
CPU TV stuff
and I2C

rising edge on ADTRIG will
start A/D "1" = 1.0 to 3.6V

TOUCH_X0 — TSX1
TOUCH_X1 — TSX2
TOUCH_Y0 — TSY1
TOUCH_Y1 — TSY2
ADTRIG IN
ADIN5 (NC), ADIN6, ADIN7
TSREF OUT — C56 2.2uF
SPIVCC IN (2.775V_BOOT)
MISO, MOSI, CLK IN, CS IN (SPI1_MISO, SPI1_MOSI, SPI1_CLK, SPI1_SS0_PMIC)
VBUSEN IN
UVBUS (NC)
VINUSB (??? POWER)
VUSB 100 mA (3.3V_USB_MX51)
UID (NC)
LICELL — C10; C163 .1 uF

May need UID if
using USB OTG

C41 2.2uF

MODE IN — Straping for Power sequence
PUMS1 IN (VCORE_DIG), PUMS2 IN (NC)
PWRON1 IN, PWRON2 IN (PMIC_ON_OD), PWRON3 IN (NC) — Internal PU to VCORE_DIG
STANDBY IN (PMIC_STBY_REQ1.8V)
STANDBYSEC IN
WDI IN (W_DOG#)
RESETBMCU OUT (POR#), RESETB OUT (RESET_IN#), INT OUT (INT_FROM_PMIC) — Both OD Need PU to 1.8V

2.775V_BOOT — R58 2.4K — Idle state is high

R46 6.04K (POWER), R47 6.04K, R37 6.04K

CLK32K — NC
CLK32KMCU OUT (CPU_32KHZ) — 1.2V level
VSRTC 50 uA (1.2V_RTC) — C59 1 uF

GPO1 OUT, GPO2 (NC), GPO3 (NC), GPO4 (NC)

SWLEDOUT (NC), LEDAD (NC), LEDB, LEDG, LEDKP (NC), LEDMD (NC), LEDR

VCOREDIG (VCORE_DIG) — 1.5V — C54 2.2uF
XTAL2 (N5), XTAL1 (N6)

Power Sequece

VS_RTC	1.2V
VCORE_DIG	1.5V
VCORE	2.775V
SW2	1.225V
SW4	1.8V_DDR
VIOHI	2.775_Boot
VGEN2	3.15V_Boot
SW1	1.05V
SW3	1.2V_DIG1
VPLL	1.8V_ANA_PLL
VDIG	1.65V
VUSB, VUSB2	

VS_RTC, VCORE_DIG, and
VCORE come up together

3.3V Power Supply

up to 1500 mA

U5 ISL8009A DFN package

POWER — FB8 — C29 10 uF 6.3V
1.8V_ANA_PLL — EN — 1.4V min
VIN, SKIP, POR, RSI, PADGND, GND
SW — L2 COIL3.3UH — 3.21V nominal — TS_3.2V
FB — 800mV — 0.8V — R97 18.2K; R23 6.04K
C33 10 uF 6.3V; C34 10 uF 6.3V
TP1; TP3

Coil = LQH44PN3R3

Max. current = 1.7 Amps

Power = 4.5V to 5.25V

3.7V > BP > 4.65V

POWER — FB2 — D5 Silicon — BP
C207 10 nF, C208 10 nF, C161 .1 uF, C32 10 uF 6.3V

BP — C44 2.2uF, C43 2.2uF, C45 2.2uF, C46 2.2uF

must be placed near 4 switcher supplies
SW1_IN, SW2_IN, SW3_IN, and SW4_IN

when ON, SWBST = 5V
When off = BP-0.3

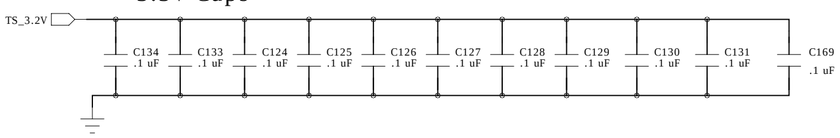
2.2 uF caps on Trans.
need series 20 milliohm

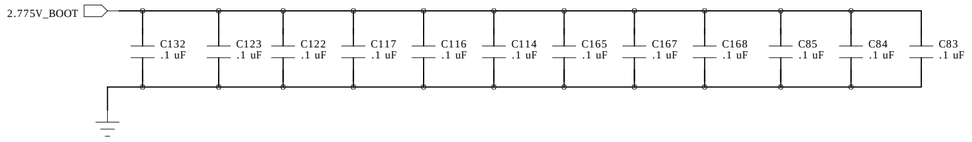
NSS12100X can handle
250 mW at 70 degrees
with min footprint

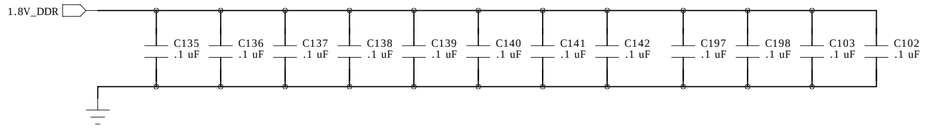
In Ref. design, 3.15V_Boot
turns on the SD2_3.3V

Technologic Systems	July 2, 2010	
Title: TS-4800 PMIC		
Rev:	Designer	Sheet 6 of 9

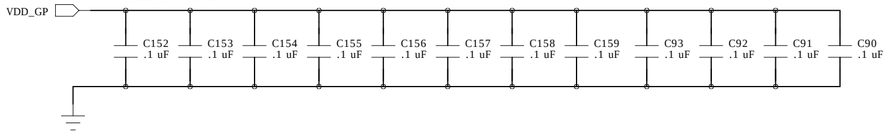
3.3V Caps



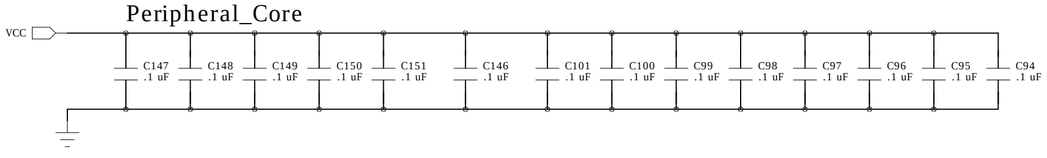


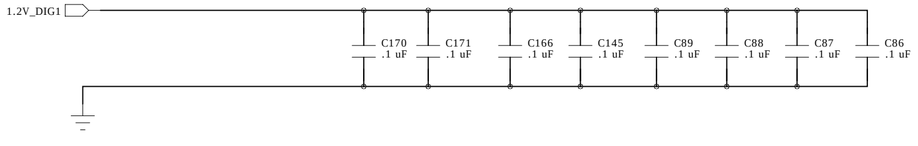


CPU Core

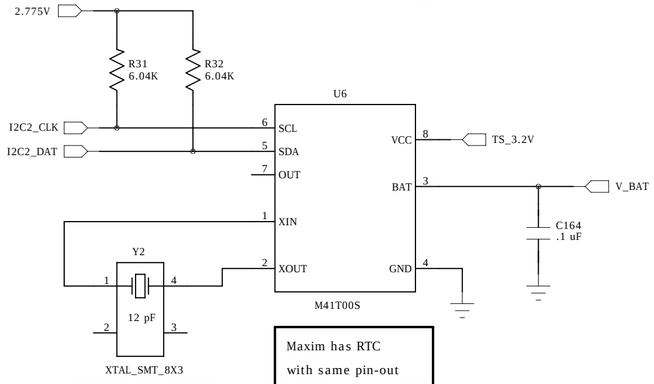


Peripheral_Core





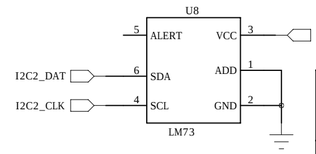
RTC



Maxim has RTC
with same pin-out

728-1005-2-ND
12.5 pF Xtal

Temp Sensor

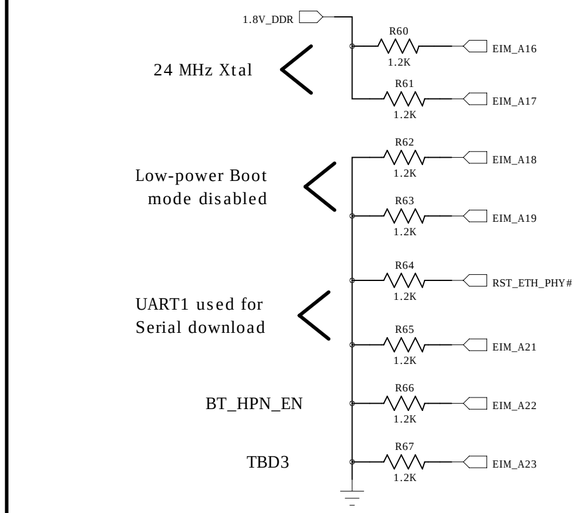


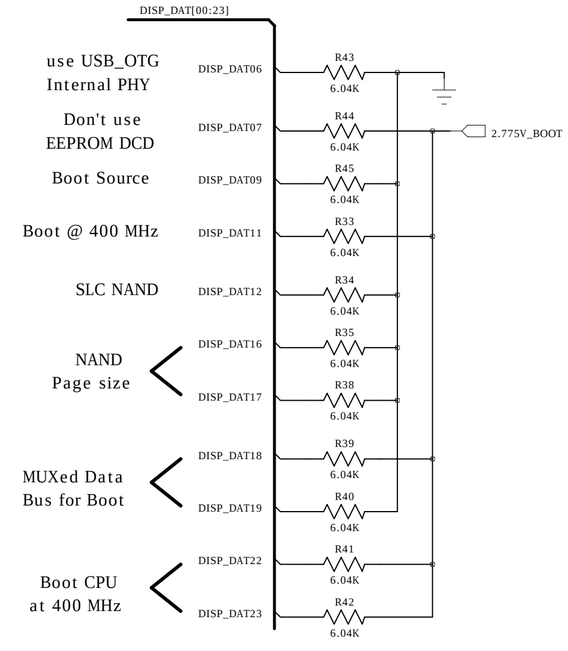
LM73CIMK-0

Zero suffix has
address at 100 1001

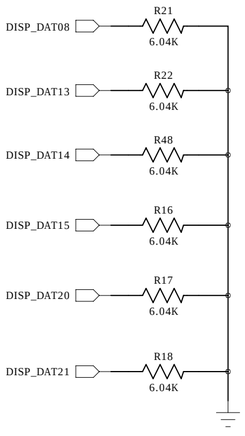
Best to Reset after
all power cycles
Set PD bit, Wait 50 mS
Then clear PD bit

Boot Strap Bias Resistors





Boot Strap Resistors



DAT_08 = Boot Source

DAT13 and DAT14
= BT_MEM_CTL

DAT15 = BT_BUS_WIDTH

DAT20 and DAT21
Boot Memory Type

Technologic Systems		July 2, 2010
Title: TS-4800 Temp, RTC, Caps, Boot_Strap		
Rev:	Designer	Sheet 7 of 9

iMX515

U10-E

1.8V_DIG1 and 1.8V_DDR are tied together on Babbage-3

All power pins should have
a .1 uF cap nearby

NVCC_I2C has 3.3V max
1.95 to 2.70V is illegal range

All have 3.1V Max.

- NVCC_EMI1 thru EMI6
- NVCC_PER3
- NVCC_PER5
- NVCC_PER8 thru PER14
- NVCC_IPUx
- NVCC_HS4_1
- NVCC_HS4_2
- NVCC_HS6
- NVCC_HS10

All have 3.6V Max.

- NVCC_PER15 = SD Card1
- NVCC_PER17 = SD Card2
- NVCC_NANDx = Flash

1.8V_DDR → T6 NVCC_EMI_DRAM_9, R6 NVCC_EMI_DRAM_8, P6 NVCC_EMI_DRAM_7, N6 NVCC_EMI_DRAM_6, M6 NVCC_EMI_DRAM_5, L6 NVCC_EMI_DRAM_4, K6 NVCC_EMI_DRAM_3, J6 NVCC_EMI_DRAM_2, H6 NVCC_EMI_DRAM_1

TS_3.2V → F5 NVCC_NANDF_A_2, E6 NVCC_NANDF_A_1, G9 NVCC_NANDF_B, G10 NVCC_NANDF_C — 3.6V Max

2.775V → T14 NVCC_I2C — 3.3V Max.

1.8V_DDR → V7 NVCC_EMI_6, U12 NVCC_EMI_5, U11 NVCC_EMI_4, U10 NVCC_EMI_3, U9 NVCC_EMI_2, U8 NVCC_EMI_1

M18 NVCC_HS4_1

U18 NVCC_PER3, G11 NVCC_PER11, U13 NVCC_PER14

2.775V_BOOT → G15 NVCC_PER5, H16 NVCC_PER8, H10 NVCC_PER9, H11 NVCC_PER10, G12 NVCC_PER12, G13 NVCC_PER13

For FEC

1.8V_DDR → R18 NVCC_IPU9, P18 NVCC_IPU8, K17 NVCC_IPU7, J17 NVCC_IPU6, H17 NVCC_IPU5, G16 NVCC_IPU4, T18 NVCC_IPU2

N18 NVCC_HS4_2, M17 NVCC_HS6, M16 NVCC_HS10

FB4, 2.775V, C113 .1 uF

TS_3.2V → G14 NVCC_PER17 — 3.6V Max

AA18 AHVDDRGB_2, Y18 AHVDDRGB_1

FB3, 1.8V_ANA_PLL, C115 .1 uF, C118 .1 uF

V6 VDD_ANA_PLL_A, W19 VDD_ANA_PLL_B — 1.95V Max

1.2V_DIG1 → U6 VDD_DIG_PLL_A, W18 VDD_DIG_PLL_B

T13 VDDA_6, P16 VDDA_5, M8 VDDA_4, H12 VDDA_3, H8 VDDA_2, G8 VDDA_1

FB10, 2.775V, C112 .1 uF

TS_3.2V → H15 NVCC_PER15 — 3.6V Max

R7 VDD_FUSE (Write only) — 3.3V Max

V16 TVDAC_DHVDD

2.775V → U16 NVCC_TV_BACK

FB5, 2.6V, C111 .1 uF, C40 2.2uF

L17 NVCC_USBPHY — 22 mA max.

3.3V_USB_MX51 → L18 VDDA33 — 8 mA max. — 3.6V Max

1.2V_RTC → U14 NVCC_SRTC_POW — 1.3V Max.

FB6, 2.6V, C110 .1 uF

W17 NVCC_OSC — 2.75V Max

? NC K21 VREG

3.0V to 3.3V max. (60 mA)

Recommended that VDD_Fuse
be floated when not writing

VDDGP_12 K7, VDDGP_11 J7, VDDGP_10 H7, VDDGP_9 G7, VDDGP_8 G6, VDDGP_7 F12, VDDGP_6 F11, VDDGP_5 F10, VDDGP_4 F9, VDDGP_3 F8, VDDGP_2 F7, VDDGP_1 F6 → VDD_GP

ARM Core Rail

nom 0.85V for < 167 MHz
nom. 1.10V for > 167 MHz

SVDDGP F13 → SENSE_VDDGP

VCC_19 T17, VCC_18 T12, VCC_17 T11, VCC_16 T10, VCC_15 T9, VCC_14 T8, VCC_13 R17, VCC_12 P17, VCC_11 P7, VCC_10 N17, VCC_9 N7, VCC_8 M7, VCC_7 L15, VCC_6 L7, VCC_5 K16, VCC_4 K15, VCC_3 J16, VCC_2 J15, VCC_1 H13 → VCC

Peripheral Supply Rail

1.05V for Low Performance mode
1.225V at High Per. (DDR @ 200 MHz)

SVCC H14 → SENSE_VCC

Must be GNDed: FASTR_ANA W20, FASTR_DIG Y20

AHVSSRGB_1 Y19, AHVSSRGB_2 AA19

NGND_USBPHY L16

NGND_TV_BACK T15

NGND_OSC V17

SGND J11

GND_DIG_PLL_B V18, GND_DIG_PLL_A T7

GND_ANA_PLL_B U17, GND_ANA_PLL_A U7

GND_62 AC23, GND_61 AC21, GND_60 AC1, GND_59 T16, GND_58 T5, GND_57 R16, GND_56 R15, GND_55 R14, GND_54 R13, GND_53 R12, GND_52 R11, GND_51 R10, GND_50 R9, GND_49 R8, GND_48 P15, GND_47 P14, GND_46 P13, GND_45 P12, GND_44 P11, GND_43 P10, GND_42 P9, GND_41 P8, GND_40 N16, GND_39 N15, GND_38 N14, GND_37 N13, GND_36 N12, GND_35 N11, GND_34 N10, GND_33 N9, GND_32 N8, GND_31 M15, GND_30 M14, GND_29 M13, GND_28 M12, GND_27 M11, GND_26 M10, GND_25 M9, GND_24 L14, GND_23 L13, GND_22 L12, GND_21 L11, GND_20 L10, GND_19 L9, GND_18 L8, GND_17 K14, GND_16 K13, GND_15 K12, GND_14 K11, GND_13 K10, GND_12 K9, GND_11 K8, GND_10 J14, GND_9 J13, GND_8 J12, GND_7 J10, GND_6 J9, GND_5 J8, GND_4 H9, GND_3 G5, GND_2 A23, GND_1 A1

IMX515

PMIC

U7-B

N11 GNDADC, B12 GNDCHRG, B9 GNDCORE, F11 GNDCTRL, D6 GNDLED, N4 GNDREG3, E2 GNDREG2, P12 GNDREG1, P6 GNDRTC, L3 GNDSPI, E6 GNDSUB1_8, E5 GNDSUB1_7, E4 GNDSUB1_6, D4 GNDSUB1_5, D3 GNDSUB1_4, B4 GNDSUB1_3, B3 GNDSUB1_2, A6 GNDSUB1_1, F6 GNDSUB2_7, F5 GNDSUB2_6, F4 GNDSUB2_5, E9 GNDSUB2_4, E8 GNDSUB2_3, E7 GNDSUB2_2, E10 GNDSUB2_1, G8 GNDSUB3_9, G7 GNDSUB3_8, G6 GNDSUB3_7, G5 GNDSUB3_6, G4 GNDSUB3_5, F9 GNDSUB3_4, F8 GNDSUB3_3, F7 GNDSUB3_2, F10 GNDSUB3_1, H8 GNDSUB4_8, H7 GNDSUB4_7, H6 GNDSUB4_6, H5 GNDSUB4_5, H3 GNDSUB4_4, G9 GNDSUB4_3, G11 GNDSUB4_2, G10 GNDSUB4_1

GNDSUB5_6 J7, GNDSUB5_5 J6, GNDSUB5_4 J5, GNDSUB5_3 H9, GNDSUB5_2 H12, GNDSUB5_1 H10

GNDSUB6_7 K7, GNDSUB6_6 K6, GNDSUB6_5 K5, GNDSUB6_4 K4, GNDSUB6_3 J9, GNDSUB6_2 J8, GNDSUB6_1 J10

GNDSUB7_6 L6, GNDSUB7_5 L5, GNDSUB7_4 L4, GNDSUB7_3 L10, GNDSUB7_2 K8, GNDSUB7_1 K10

GNDSUB8_5 P9, GNDSUB8_4 P8, GNDSUB8_3 P7, GNDSUB8_2 P5, GNDSUB8_1 P10

GNDSW1_2 G14, GNDSW1_1 G13

GNDSW2_2 K14, GNDSW2_1 K13

GNDSW3_2 G2, GNDSW3_1 G1

GNDSW4_2 K2, GNDSW4_1 K1

GNDSWBST D5, GNDSWLED D8

Technologic Systems		July 2, 2010
Title: TS-4800 Power		
Rev:	Designer	Sheet 8 of 9

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.25V to these pins

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7, OFF_BD_RESET# 9

OFF_BD_RESET# is an Output
used to reset all peripherals

11, NC 13, POWER 15, NC 17, 19

DISP_DAT08 21, DISP_DAT09 23, DISP_DAT10 25, DISP_DAT11 27, DISP_DAT12 29, POWER 31, DISP_DAT13 33, DISP_DAT14 35, DISP_DAT15 37, DISP_DAT16 39, DISP_DAT17 41, DISP_DAT18 43, DISP_DAT19 45, DISP_DAT20 47, POWER 49, DISP_CLK 51, DISP_HSYNC 53, DISP_VSYNC 55, DISP_DE 57, LCD_PWM 59, 61

DIO_[00:16]

FPGA DIO: DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, 75, DIO_08 77, DIO_07 79, DIO_06 81, DIO_05 83, DIO_04 85, DIO_03 87, DIO_02 89, DIO_01 91, DIO_00 93, 95

BUS_WAIT# 97, BUS_BHE# 99

2 EXT_RESET#, 4 EN_USB_5V

Off-Bd SD Card: 6 SD1_D2, 8 SD1_D3, 10 SD1_CMD, 12 SDCARD_3.2V, 14 SD1_CLK, 16 POWER, 18 SD1_D0, 20 SD1_D1

22, 24 DISP_DAT00, 26 DISP_DAT01, 28 DISP_DAT02, 30 DISP_DAT03, 32 DISP_DAT04, 34 DISP_DAT05, 36 V_BAT, 38 DISP_DAT06, 40 DISP_DAT07, 42 DISP_DAT21, 44 DISP_DAT22, 46 DISP_DAT23, 48 EN_LCD_3.3V, 50, 52, 54, 56, 58, 60, 62

Data Bus: 64 MUX_AD_15, 66 MUX_AD_14, 68 MUX_AD_13, 70 MUX_AD_12, 72 MUX_AD_11, 74 MUX_AD_10, 76 MUX_AD_09, 78 MUX_AD_08, 80 MUX_AD_07, 82 MUX_AD_06, 84 MUX_AD_05, 86 MUX_AD_04, 88 MUX_AD_03, 90 MUX_AD_02, 92 MUX_AD_01, 94 MUX_AD_00

Bus Control: 96 BUS_ALE#, 98 BUS_DIR, 100 BUS_CS#

MUX_AD_[00:15]

TYCO_100PIN

Right

CN2

Ethernet: ETH_RX+ 1, ETH_RX- 3, ETH_CT 5, ETH_TX+ 7, ETH_TX- 9, ETH_CT 11, TS_3.2V 13, 15

Max off-board load on
TS_3.2V is 500 mA

17, 19, 21, NC 23, NC 25, NC 27

USB Ports: HOSTA_USB_M 29, HOSTA_USB_P 31, FPGA_1.2V 33, USB_OTG_D- 35, USB_OTG_D+ 37, TS_3.2V 39, 41, 43

Maximum off-board load
on 2.775V, 1.8V, 1.2V
is 10 mA each

45, 47, 49, 51, 53, 55, 1.8V_DDR 57, 59, 61

SPI: 2.775V_BOOT 63, SPI_CS# 65, SPI_MOSI 67, SPI_MISO 69, SPI_CLK 71

73, 75, 1.8V_DDR 77, 79, 81, 83, 85, 87, 89

1.8V Level CPU DIO

Console: DIAG_LED# 91, DEBUG_TXD 93, DEBUG_RXD 95, CAN_TXD 97, CAN_RXD 99

2 ETH_LEFT_LED, 4 ETH_RIGHT_LED, 6 RED_LED#, 8 GREEN_LED#, 10, 12, 14

A/D: 16 TOUCH_X0, 18 TOUCH_X1, 20 TOUCH_Y0, 22 TOUCH_Y1

24, 26

I2C 2.775V: 28 I2C2_CLK, 30 I2C2_DAT

32 EN_232_TRANS, 34

34 AUD_MCLK = NC

CPU JTAG: 36 AUD_CLK, 38 AUD_FRM, 40 AUD_TXD, 42 AUD_RXD, 44 CPU_JTAG_TMS, 46 CPU_JTAG_TCK, 48 CPU_JTAG_TDI, 50 CPU_JTAG_TDO

52 ONE_WIRE, 54 DIO_20

54 Codec MCLK

56 GPIO1_7, 58 GPIO1_3, 60 GPIO1_5, 62 DIO_19, 64 DIO_18, 66 GPIO4_13, 68 GPIO4_14, 70 DIO_17, 72 GPIO1_6, 74 USB_OTG_ID, 76 USB_5V_LINE

Serial Ports: 78 UART0_TXD, 80 UART0_RXD, 82 UART1_TXD, 84 UART1_RXD, 86 UART2_TXD, 88 UART2_RXD, 90 UART3_TXD, 92 UART3_RXD, 94 UART4_TXD, 96 UART4_RXD, 98 UART5_TXD, 100 UART5_RXD

TYCO_100PIN

Boot Strap

Mode 2	TS-4800 Boots from
1	NAND Flash
0	SD Card

State of BUS_DIR (Mode 2)
is latched prior to
OFF_BD_RESET# deasserted

BUS_DIR = MODE2

BUS_DIR has 12K PU resistor

Connect 1.5K ohm resistor
between BUS_RD# and
OFF_BD_RESET# to set low
(Boot from SD card)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Technologic Systems	July 2, 2010
Title: TS-4800 Off-board Connectors	
Rev:	Designer / Sheet 9 of 9