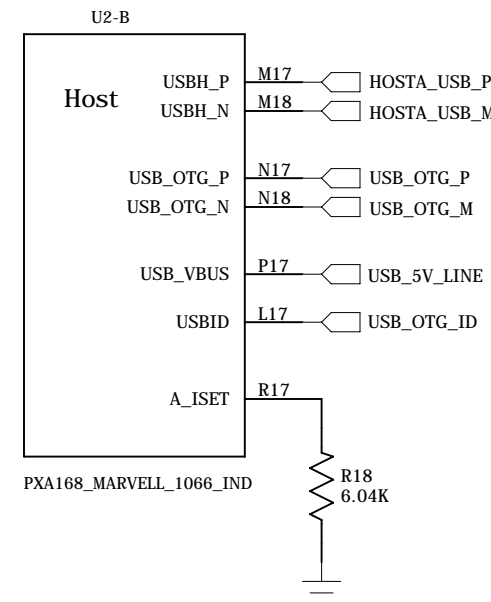
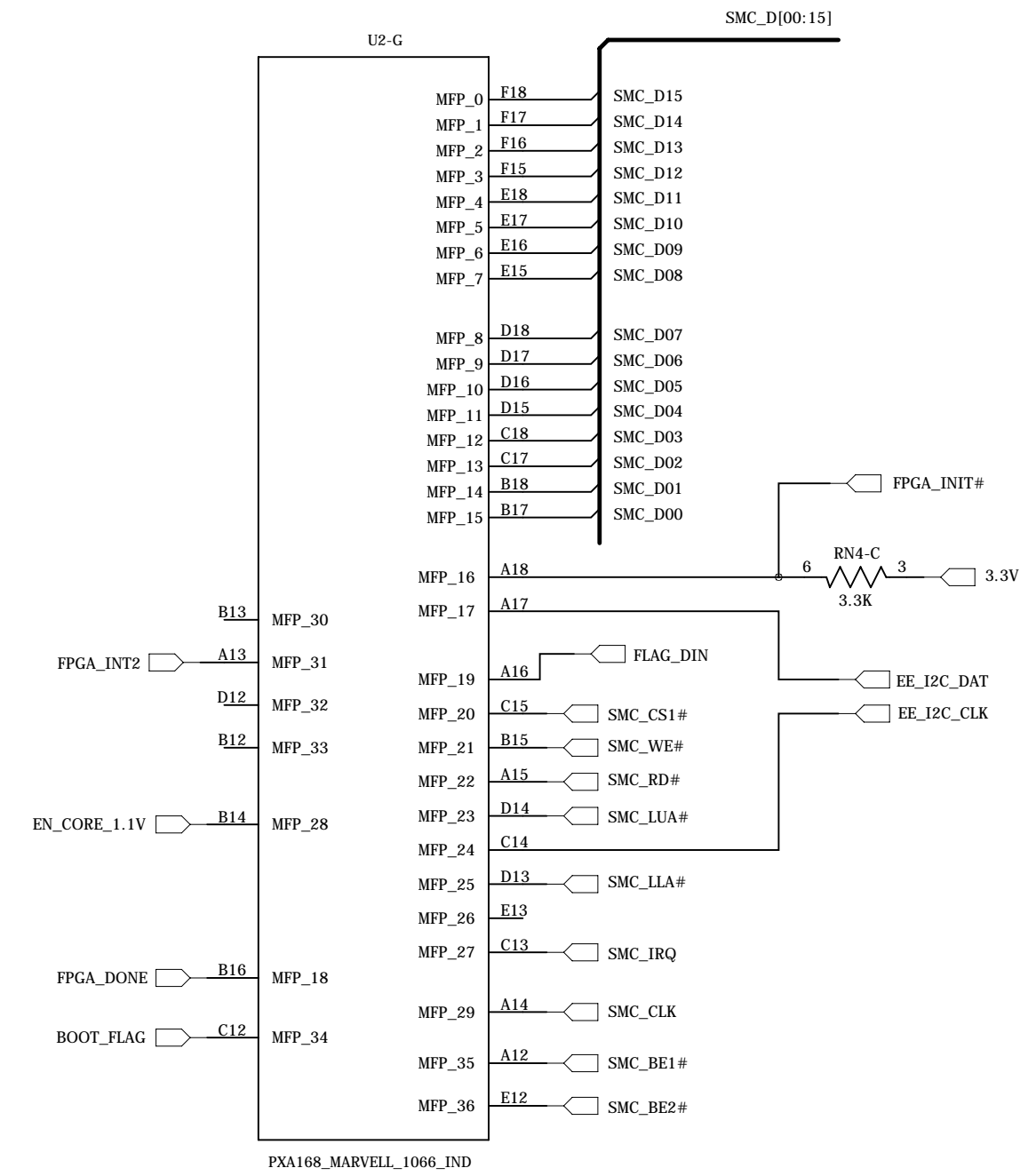


PXA168 1066 MHz

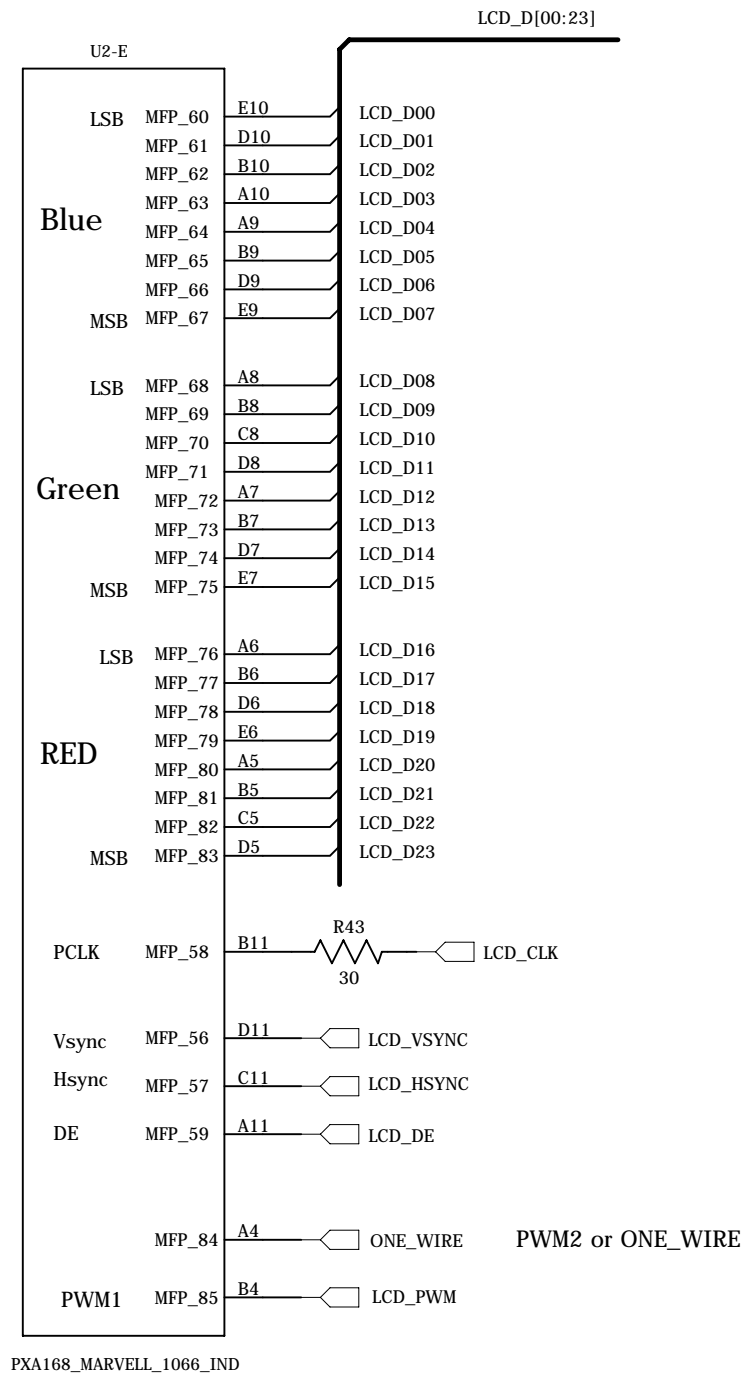
USB Ports



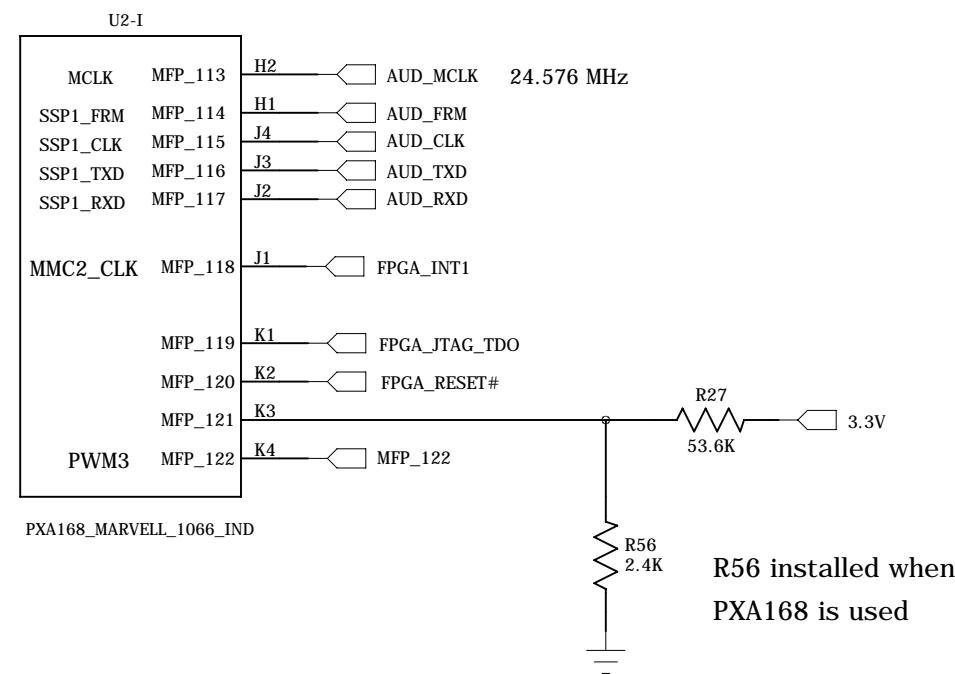
SMC Bus



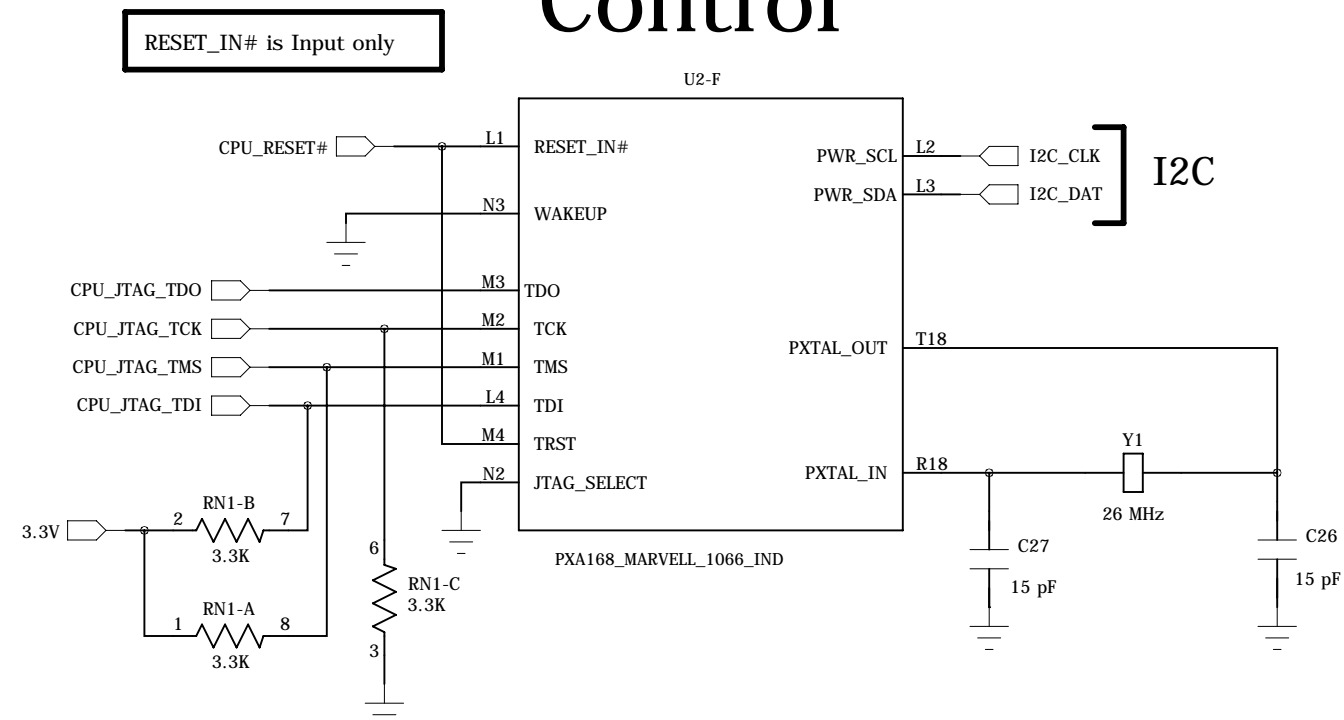
LCD



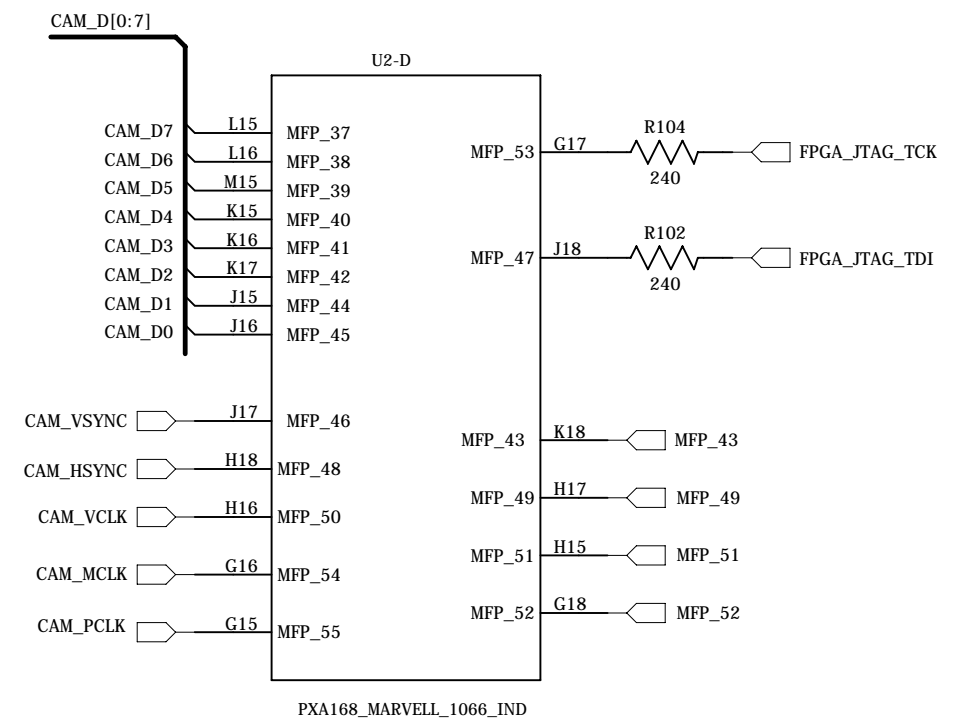
I2S



Control



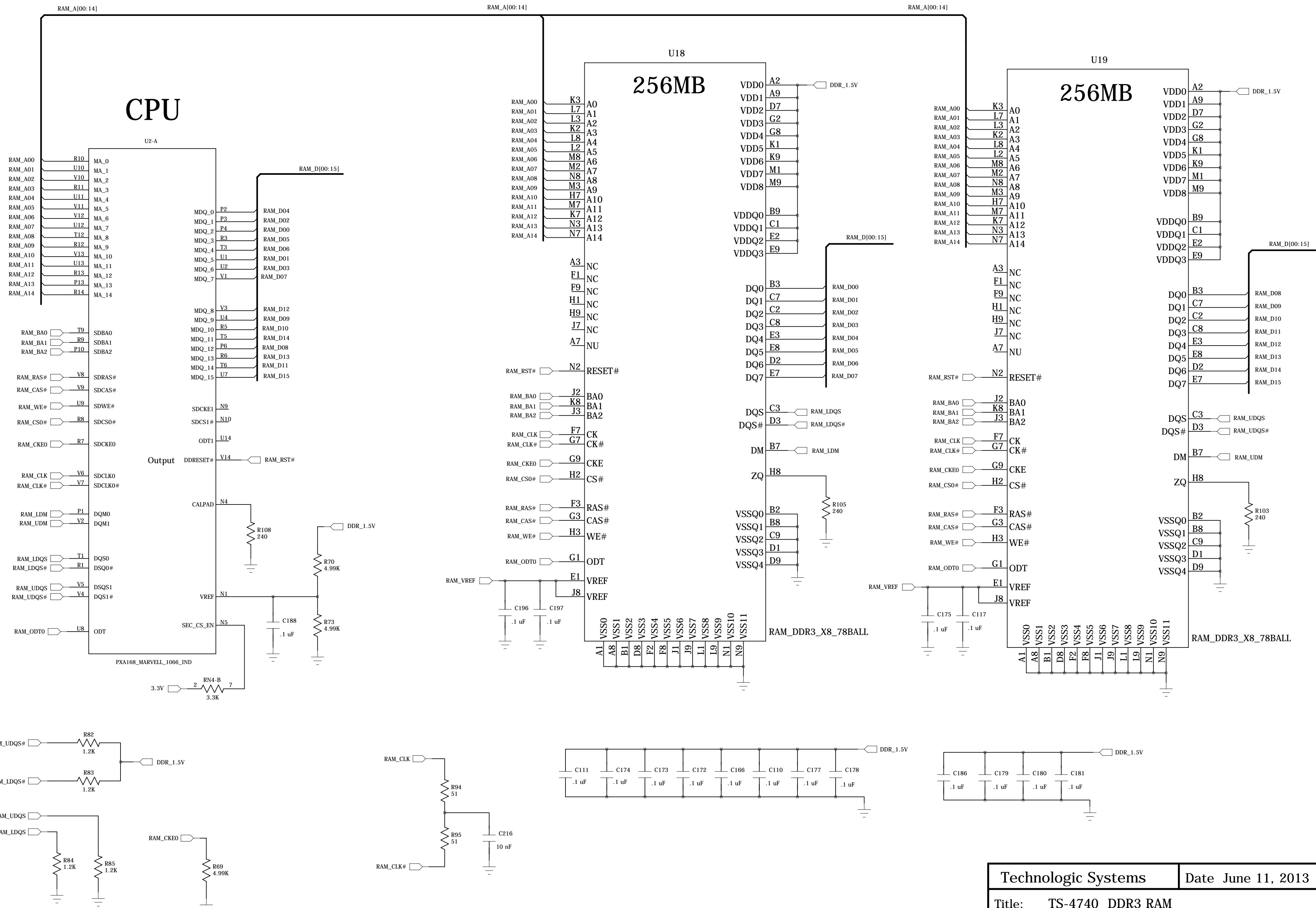
Camera



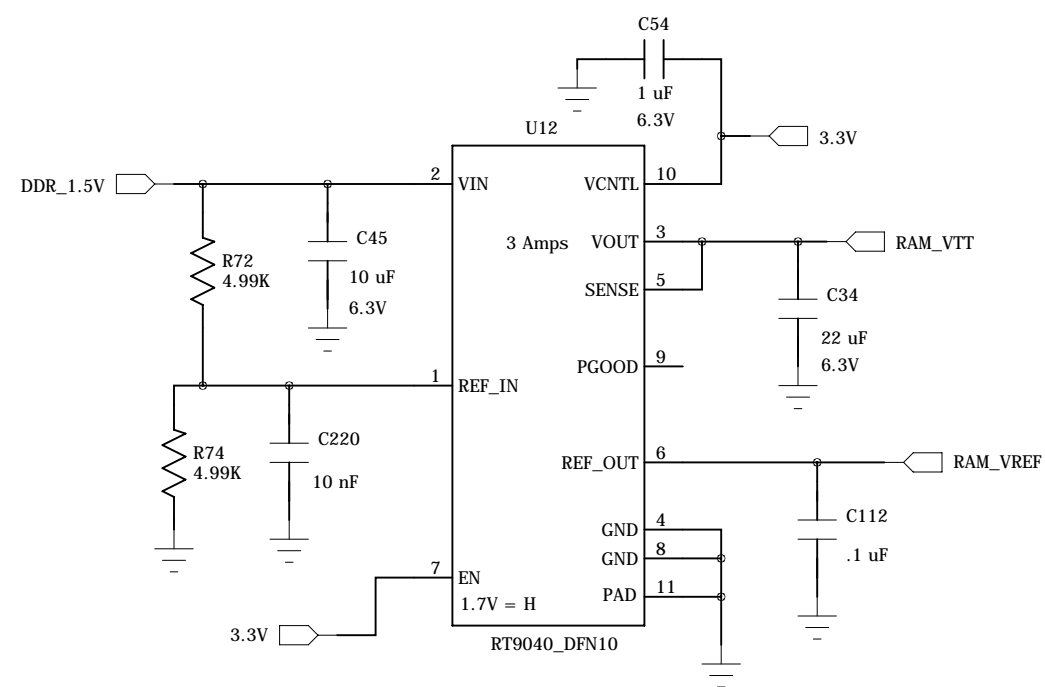
DDR3 x8 RAM

2 Gbit RAM chips

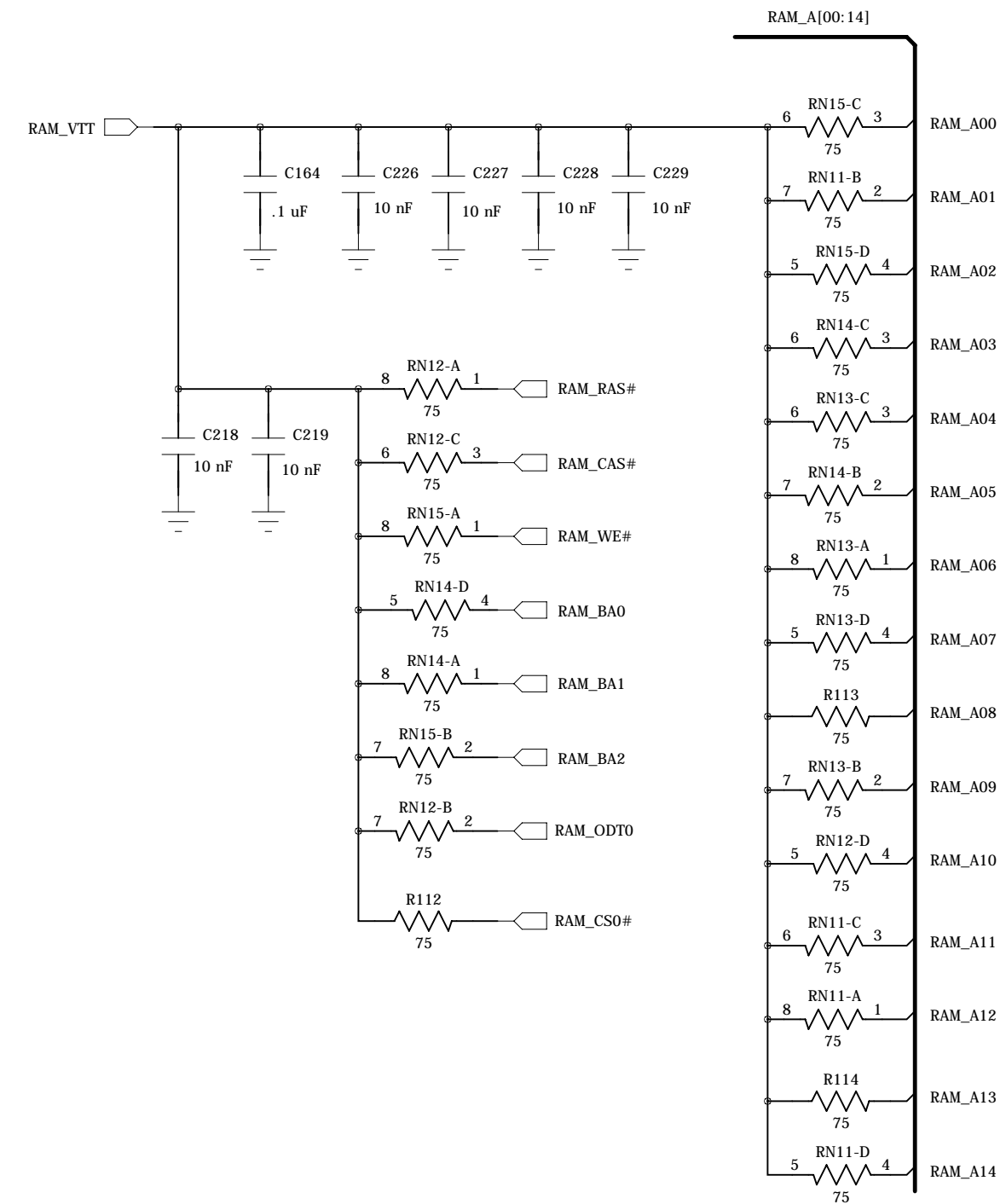
512 MB RAM Total



DDR3 RAM Termination Power Supply

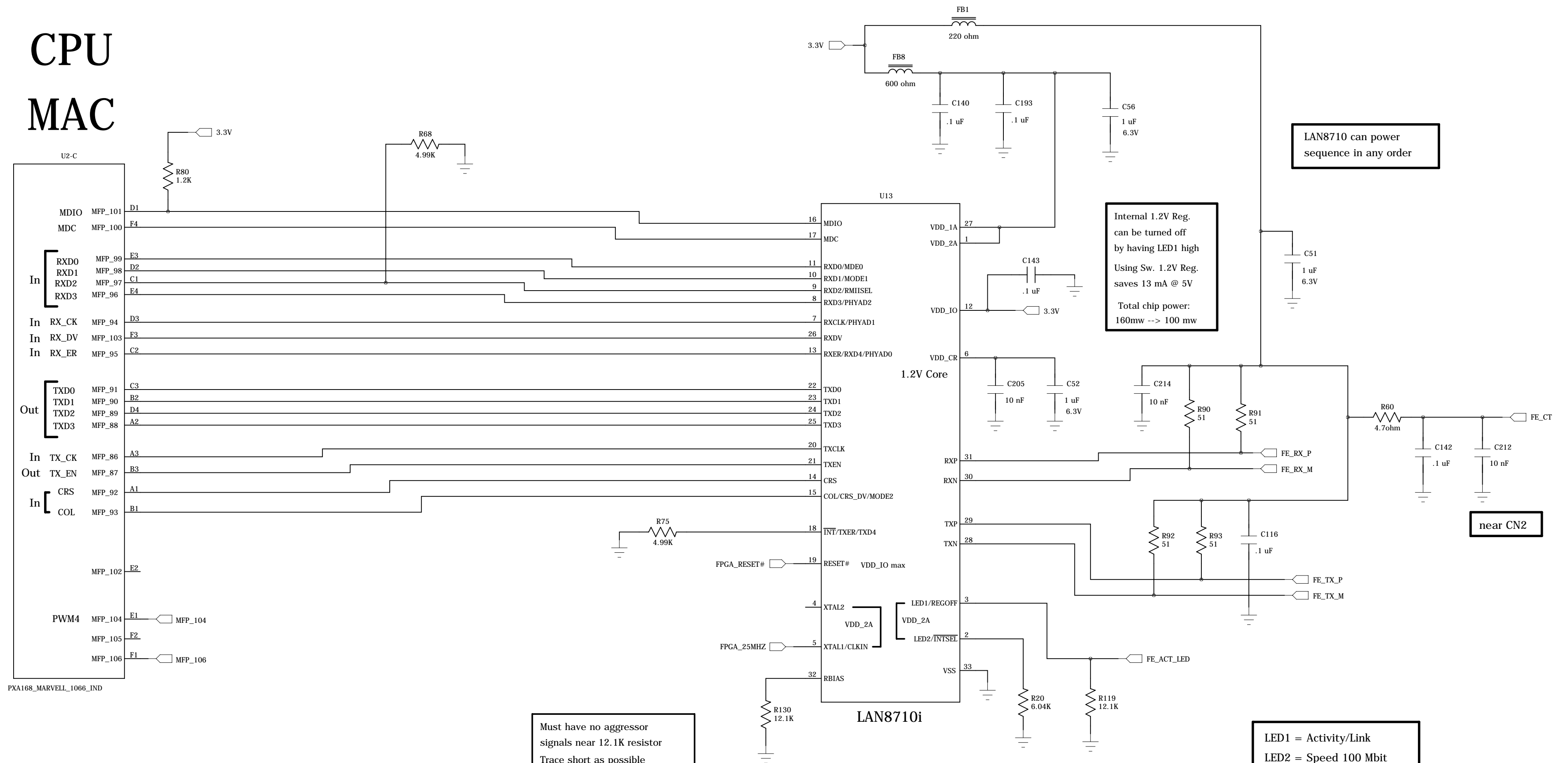


Termination Resistors



10/100 Ethernet Port

CPU
MAC



LAN8710 can power sequence in any order

Internal 1.2V Reg. can be turned off by having LED1 high
Using Sw. 1.2V Reg. saves 13 mA @ 5V
Total chip power: 160mw -> 100 mw

near CN2

Must have no aggressor signals near 12.1K resistor
Trace short as possible

PHY address = 0

LED1 = Activity/Link
LED2 = Speed 100 Mbit

MDIO bus can not be used until 100 uS after Reset# is deasserted
MDCLK max is 2.5 MHz

PHY address and modes latched on rising edge of Reset#

Put MX515 in MII mode before deasserting Reset#

LED high voltage is VDD_2A = 3.3V

PXA168_MARVELL_1066_IND

Xilinx LX25T_324 FPGA

25K equivalent LUTs
(15K 6-input LUTs)

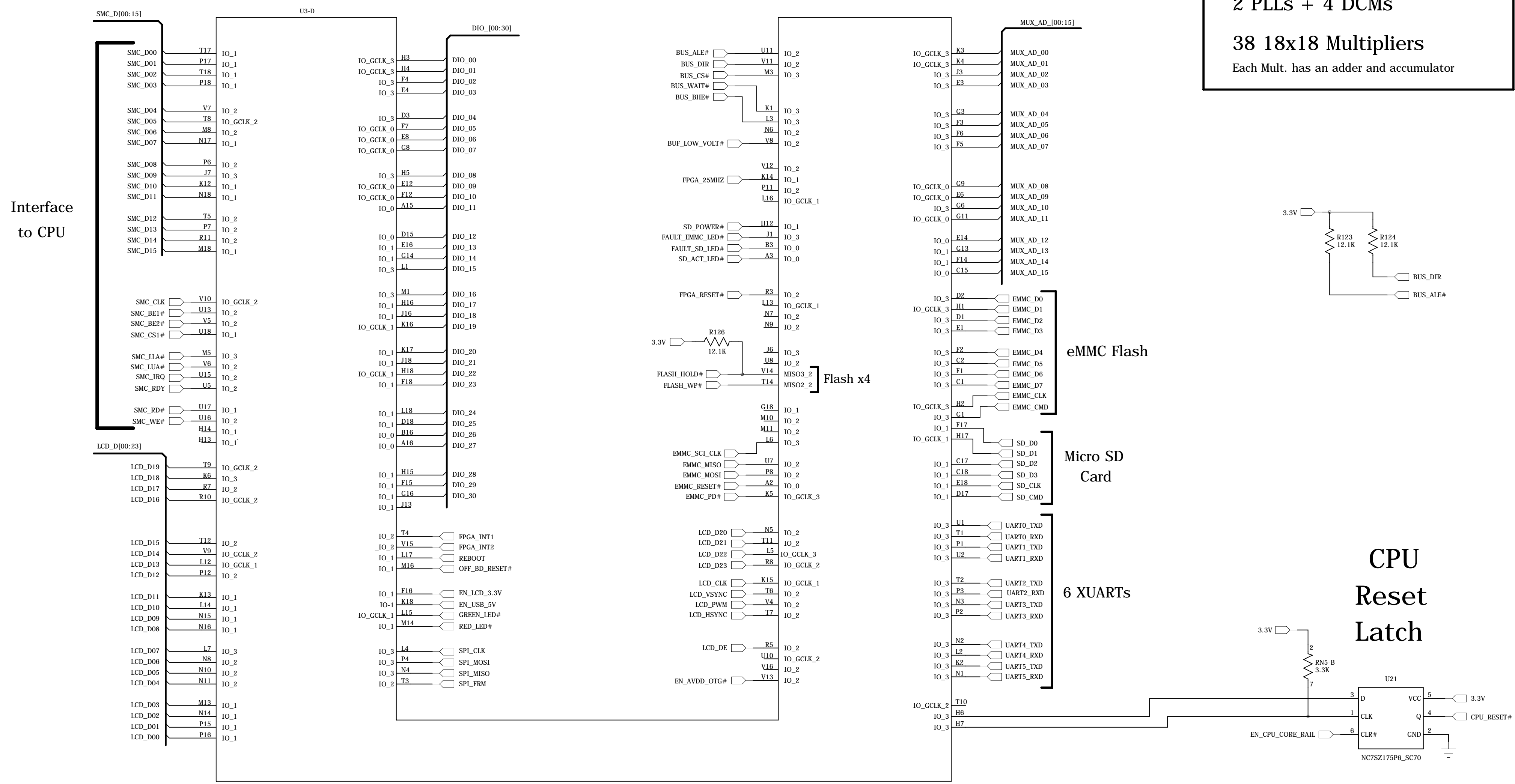
177 DIO

30K Flip-flops

52 [2K x 9] Block RAM

2 PLLs + 4 DCMs

38 18x18 Multipliers
Each Mult. has an adder and accumulator



Bit stream should initialize
EN_AVDD_OTG# deasserted (high)

After FPGA_RESET# deasserted,
It should assert EN_AVDD_OTG#

Then wait 10 ms, and write
a "1" into the CPU RESET Latch

Power up

FPGA_RESET# will still be asserted
after FPGA is configured
and can be used as a FPGA reset

CPU reload bit stream

CPU can also drive FPGA_RESET#
low during a "soft" FPGA update

REBOOT = "Cold Boot" causes
LOW_VOLT# to be asserted
This will collapse all rails and
it will assert CPU reset and
will reload FPGA from Flash

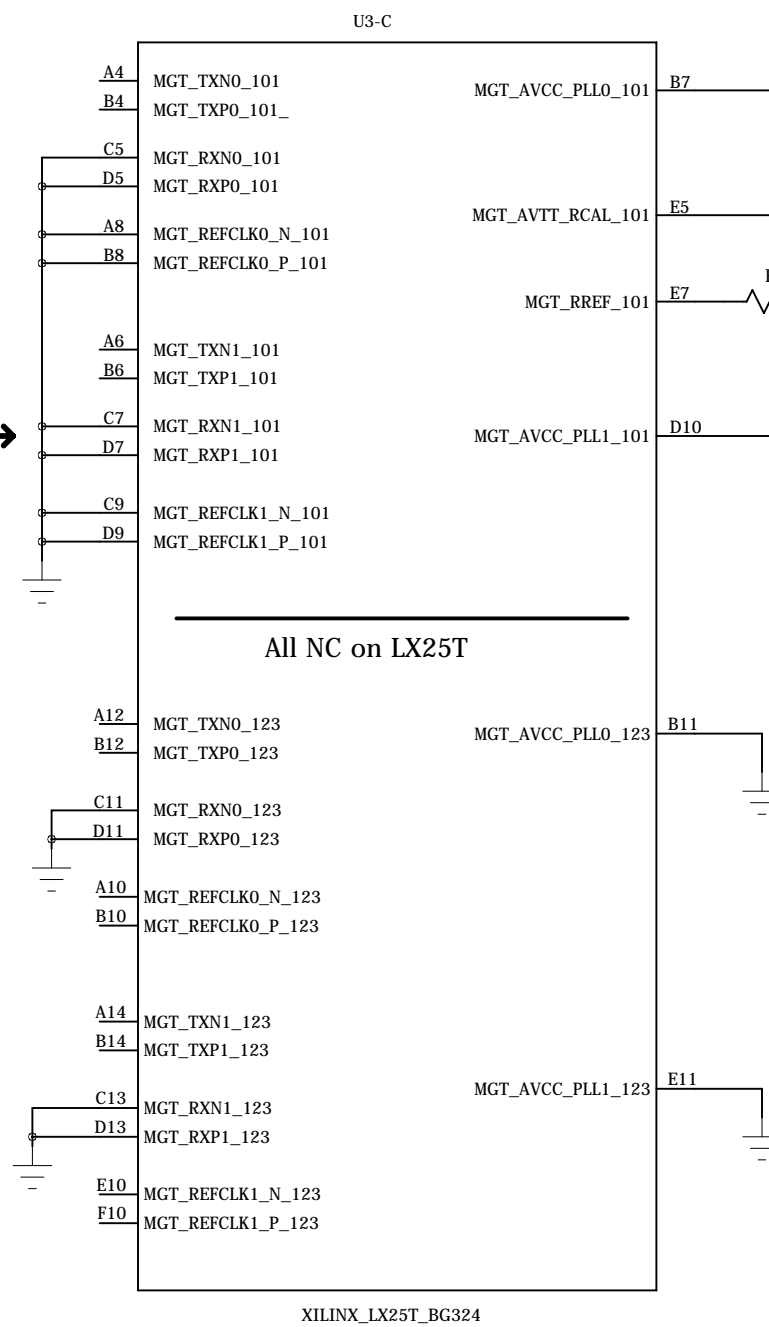
This will clear Boot Flag

"Warm Reboot" occurs
by clearing Reset Latch
This will reload the FPGA

This will not clear Boot Flag

Xilinx LX25T_324 FPGA

Gigabit Transceivers

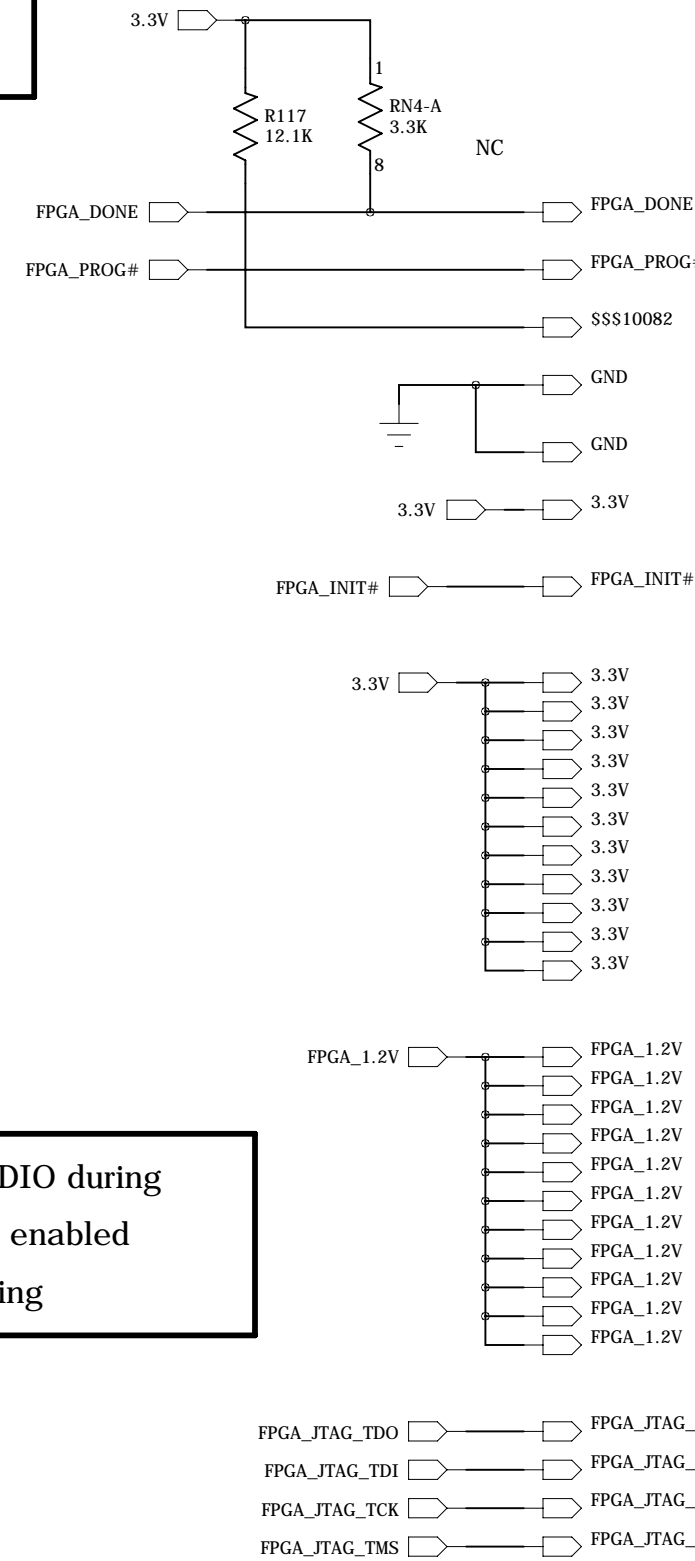


Page 162 GTP User Guide

Page 168-169
REF_CLK Inputs have
internal 100 ohm term.
must be cap coupled

FPGA_INIT# can be used
to delay configuration
Also indicates load error

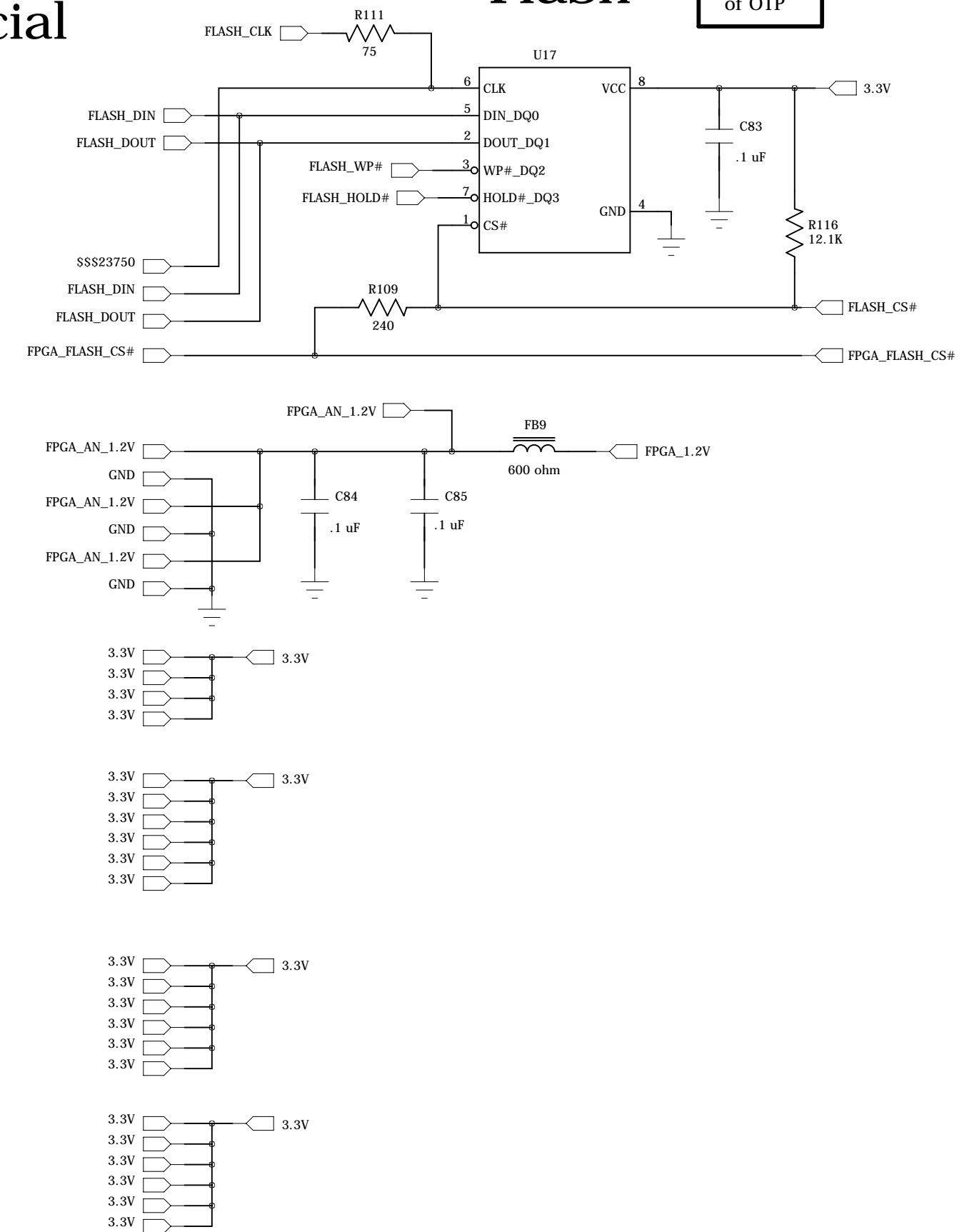
Power and Special Functions



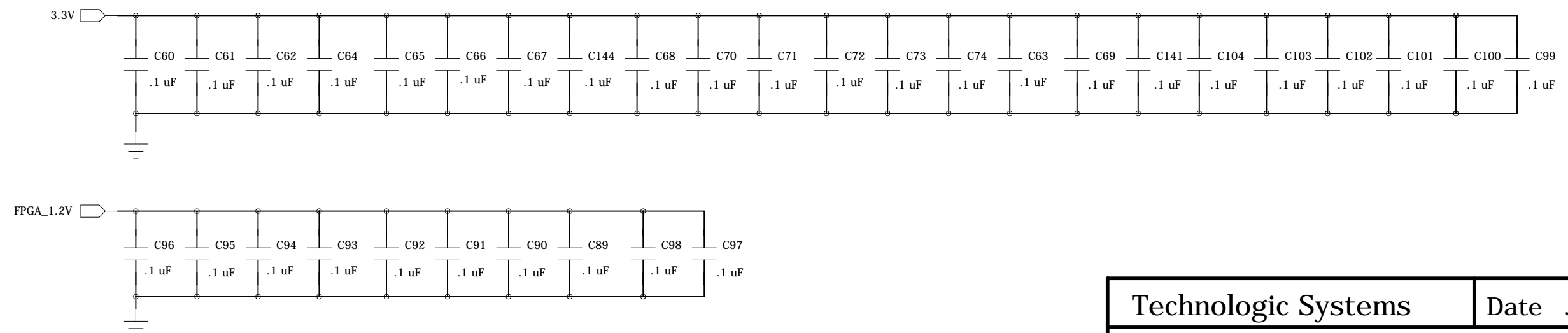
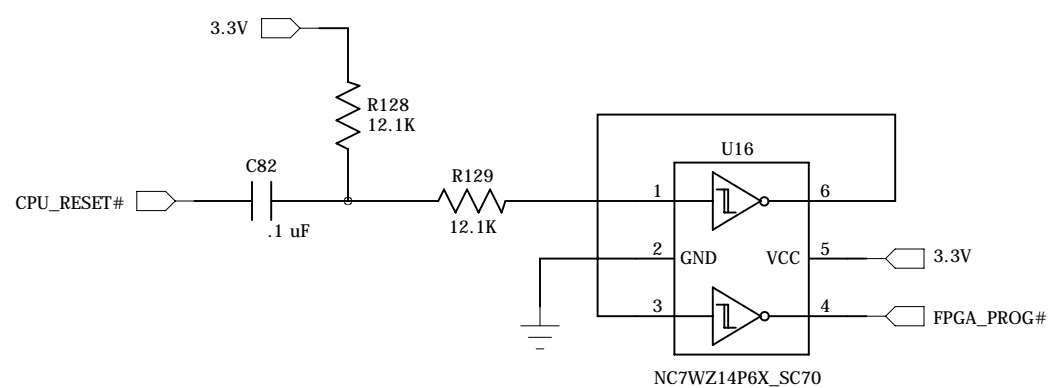
IO_SWAPEN_0 controls DIO during
configuration. Low = PU enabled
High = All DIO are floating

8MB SPI Flash

64 bytes
of OTP

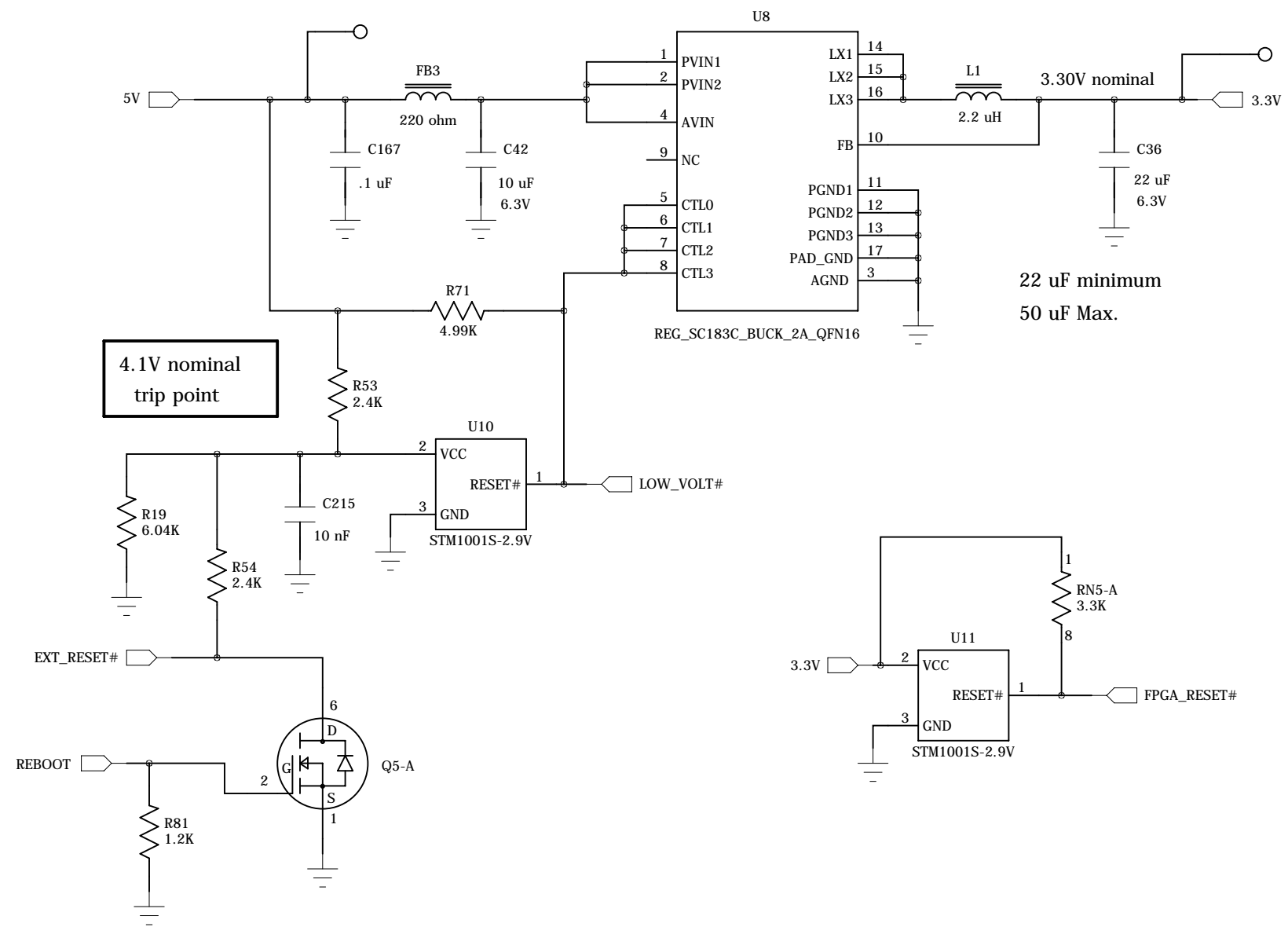


FPGA Reload



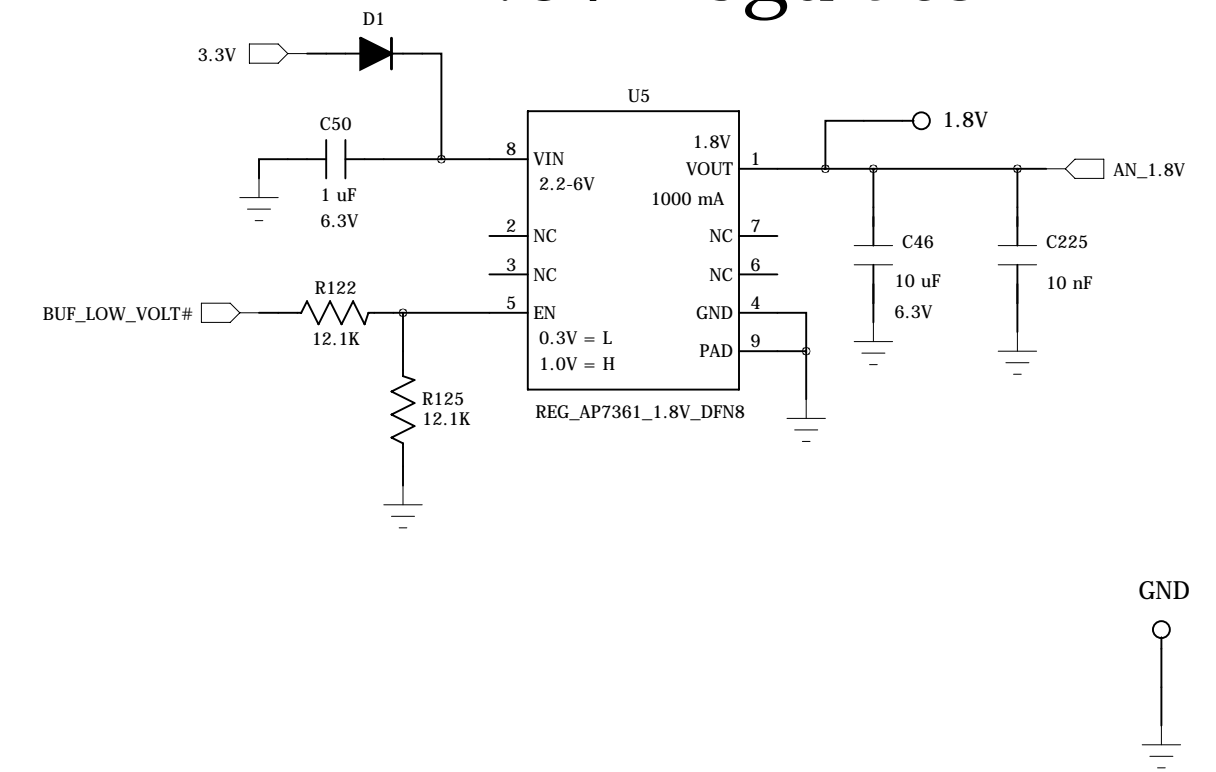
3.3V Power Supply

up to 2000 mA

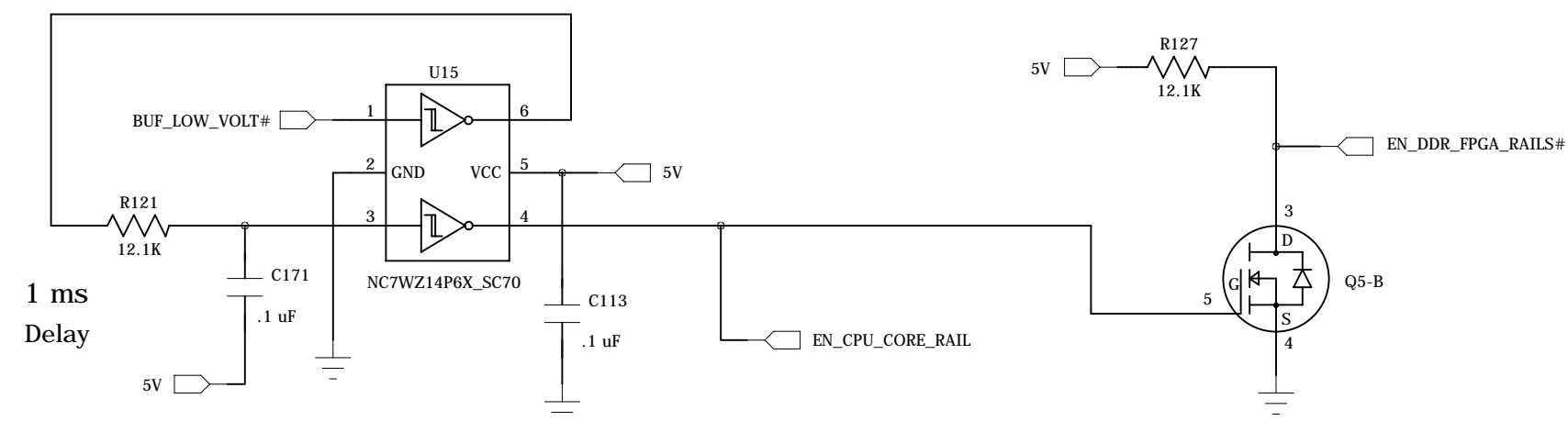


Power Supplies

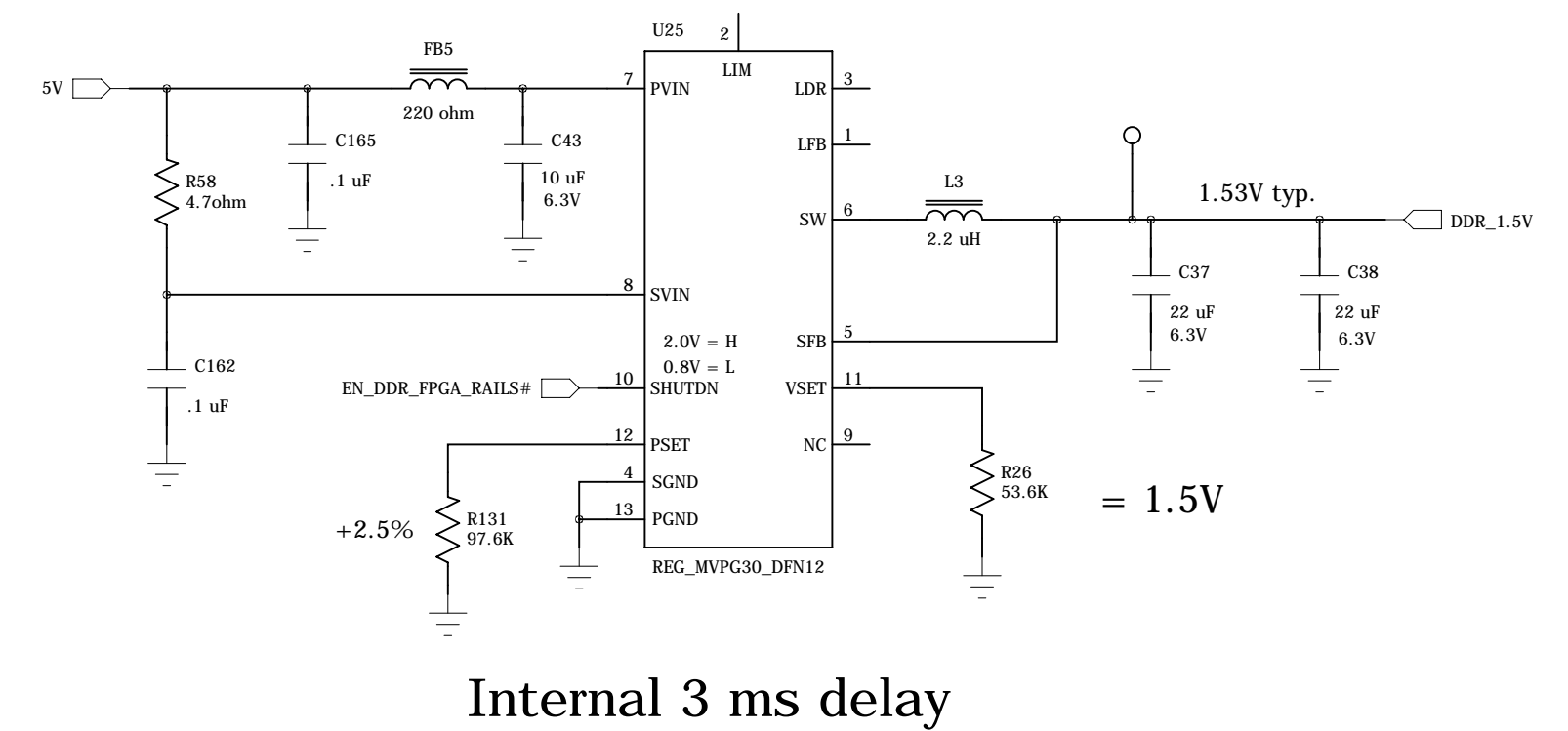
Analog 1.8V Regulator



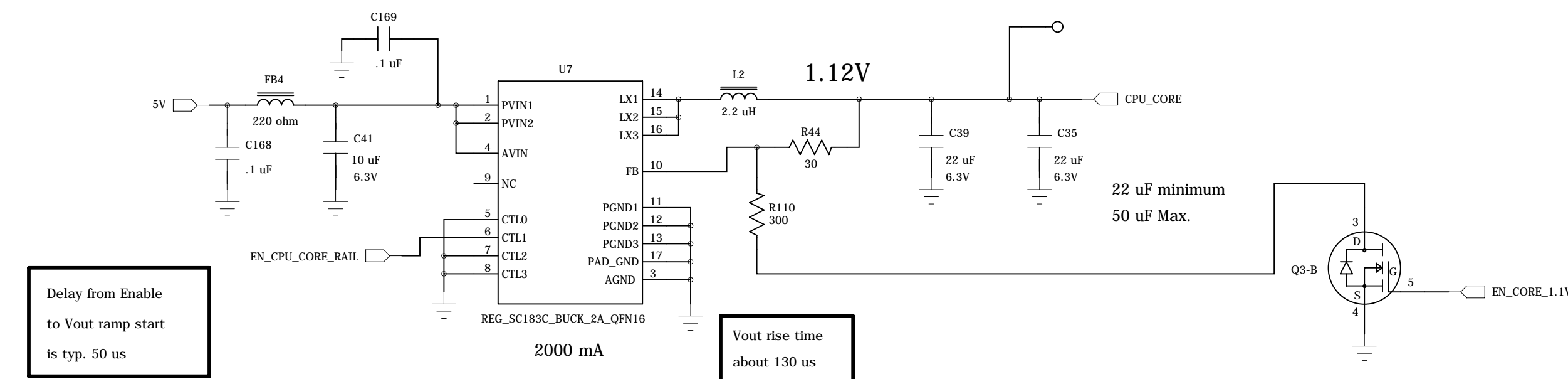
Power Sequencer



DDR3 1.5V Reg.



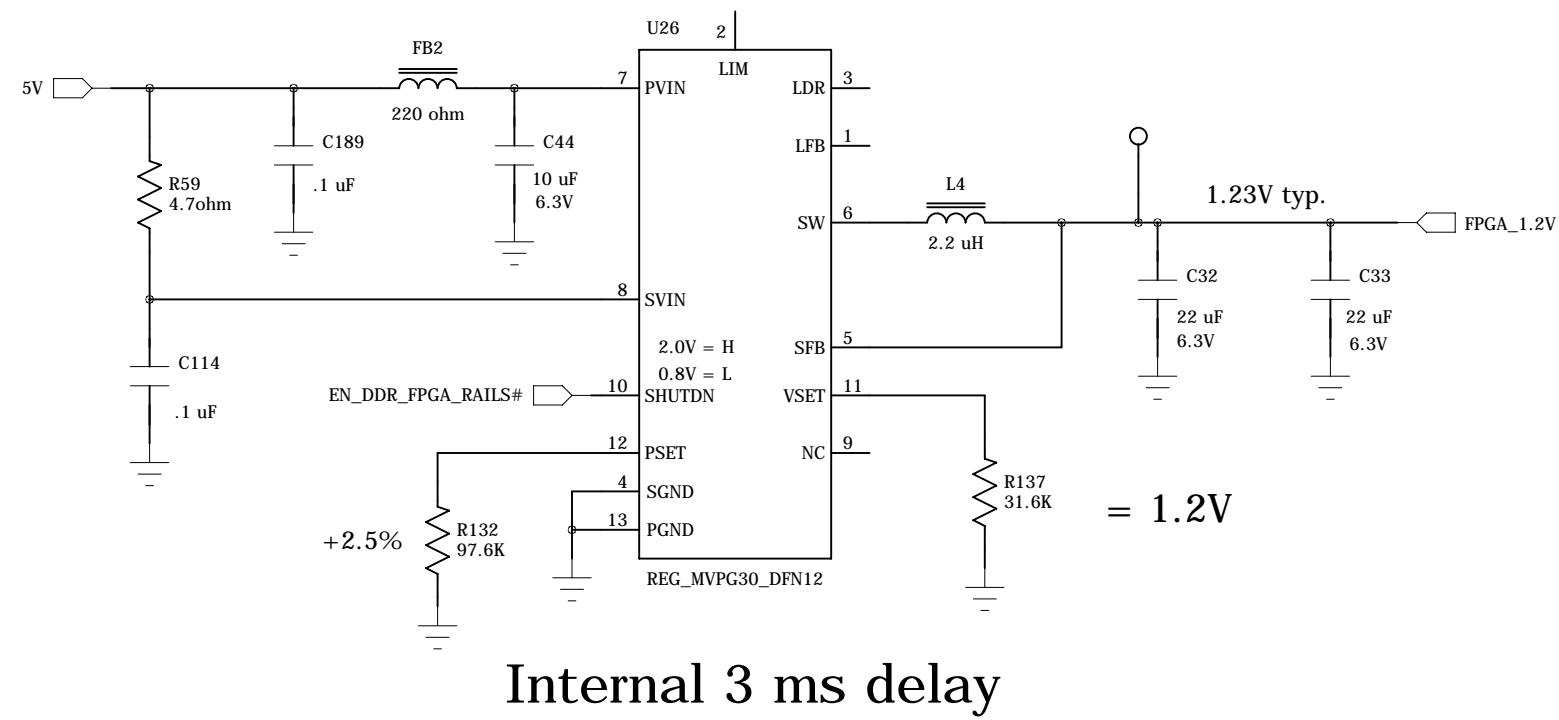
CPU Core Supply



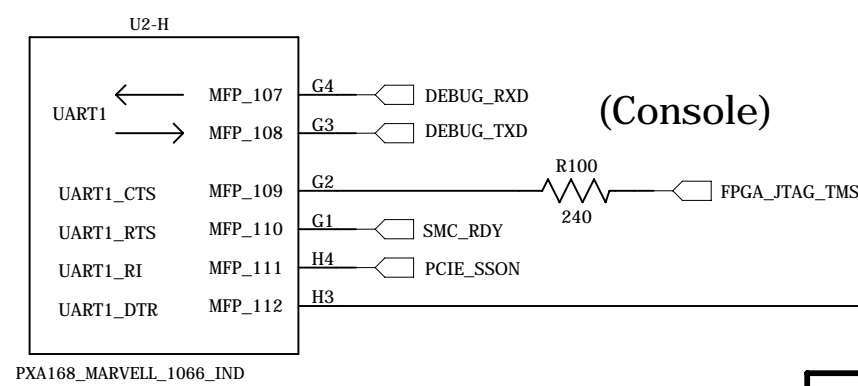
Internal 3 ms delay

Technologic Systems	Date June 11, 2013
Title: TS-4740 Power Supplies	
Rev: A	Designer
Sheet 7 of 13	

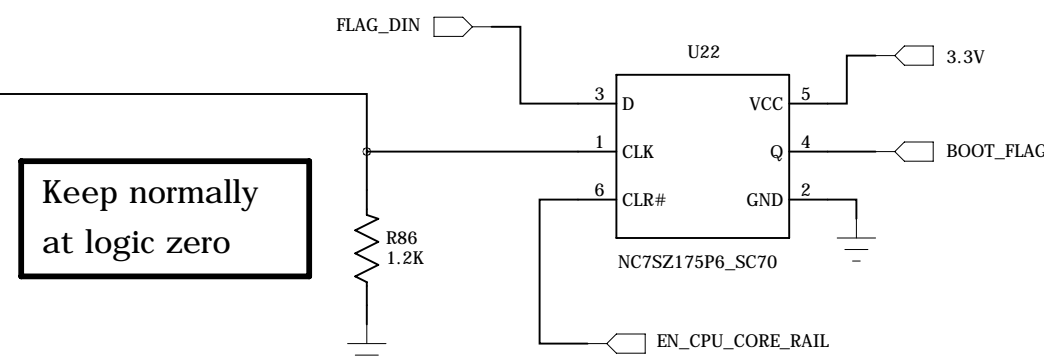
FPGA Core 1.2V



CPU Debug UART

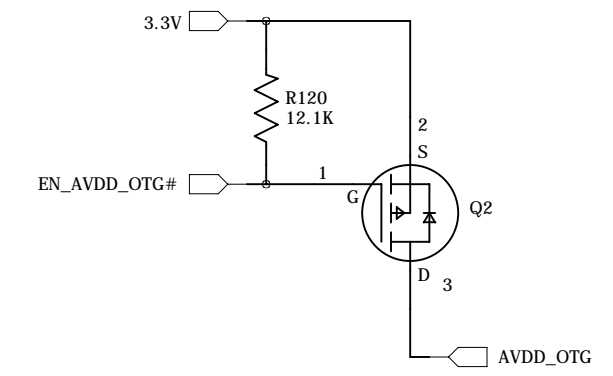


Reboot Flag



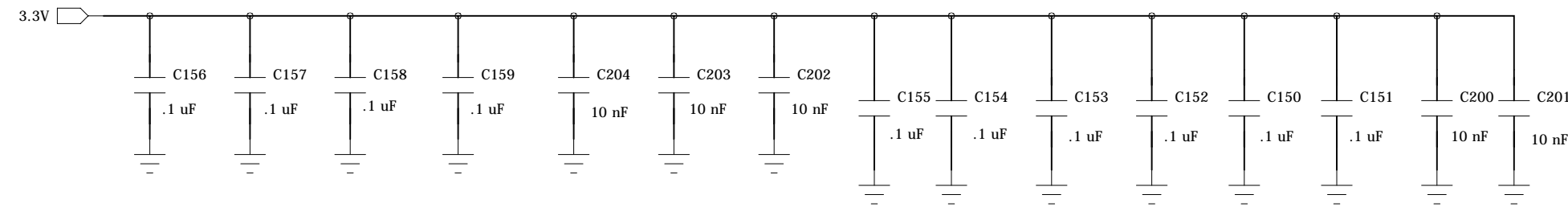
Keep normally
at logic zero

CPU USB Power

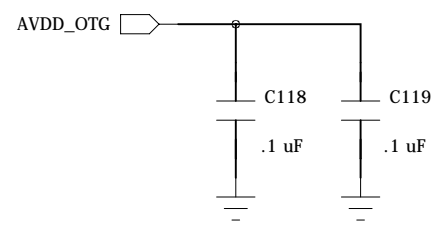
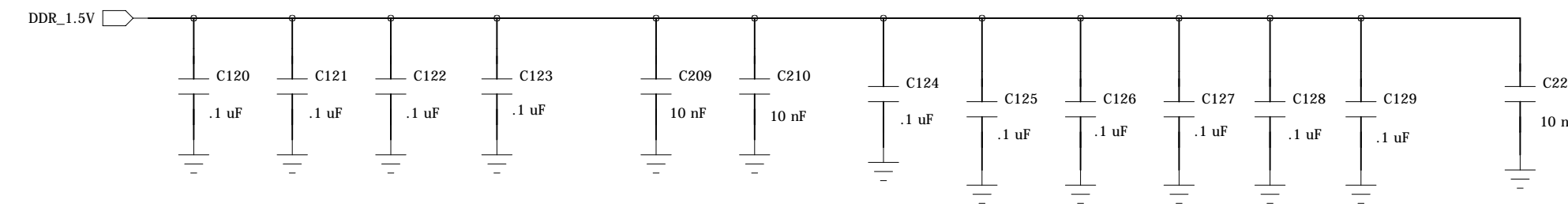
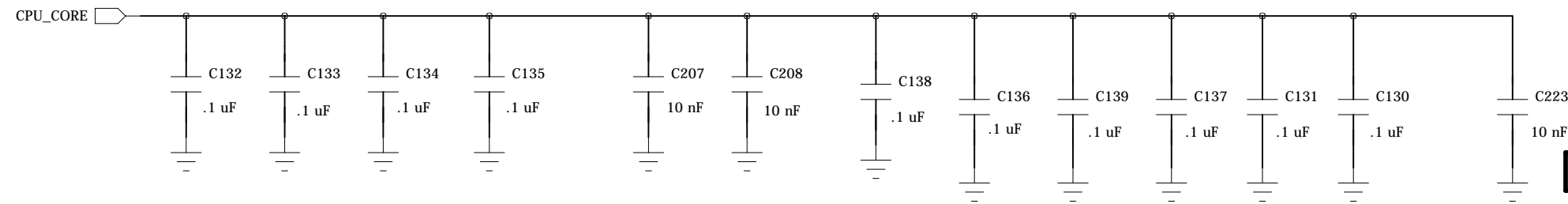
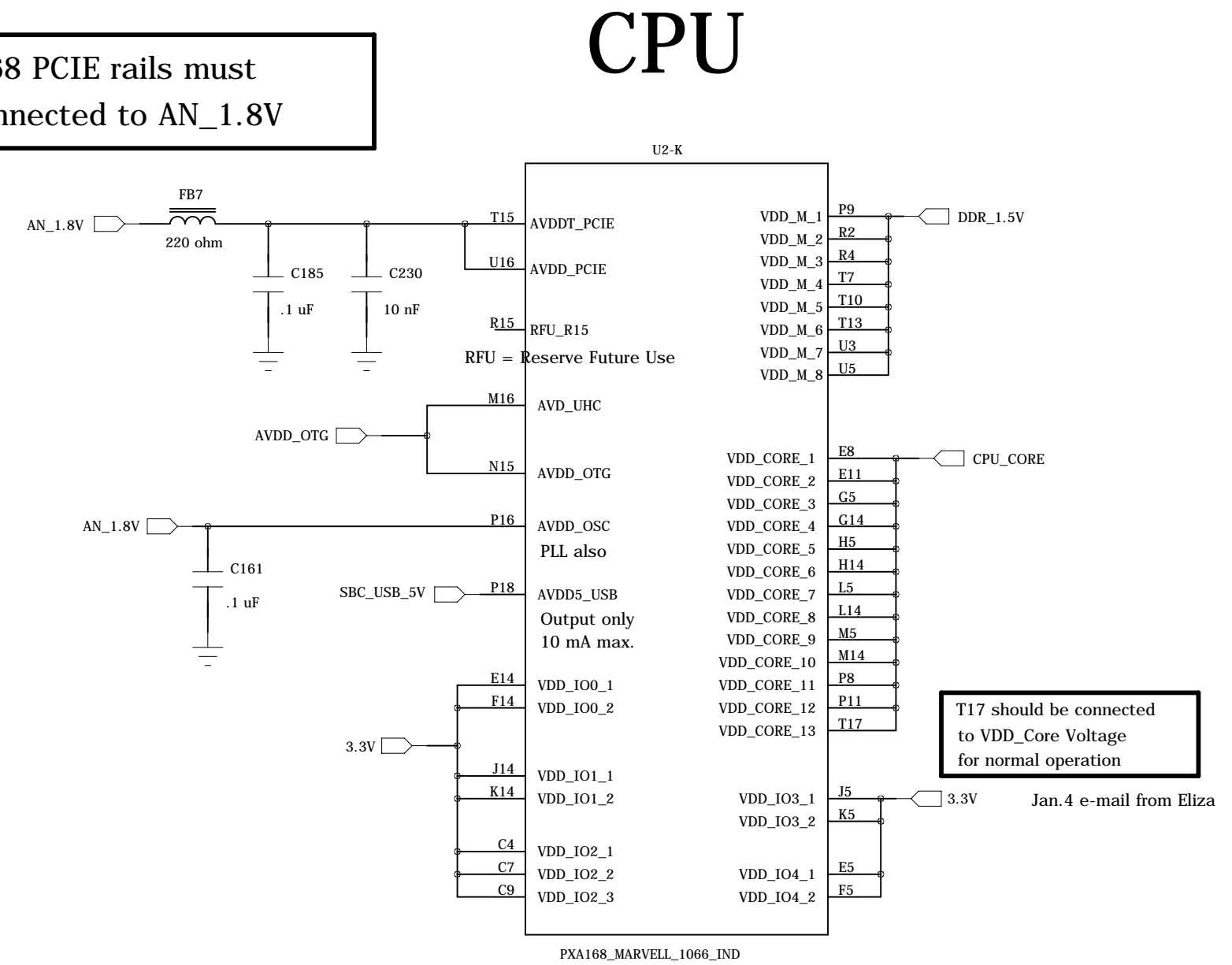


Technologic Systems		Date June 11, 2013
Title: TS-4740 FPGA 1.2V Supply, Reboot Flag		
Rev: A	Designer	Sheet 8 of 13

CPU Power

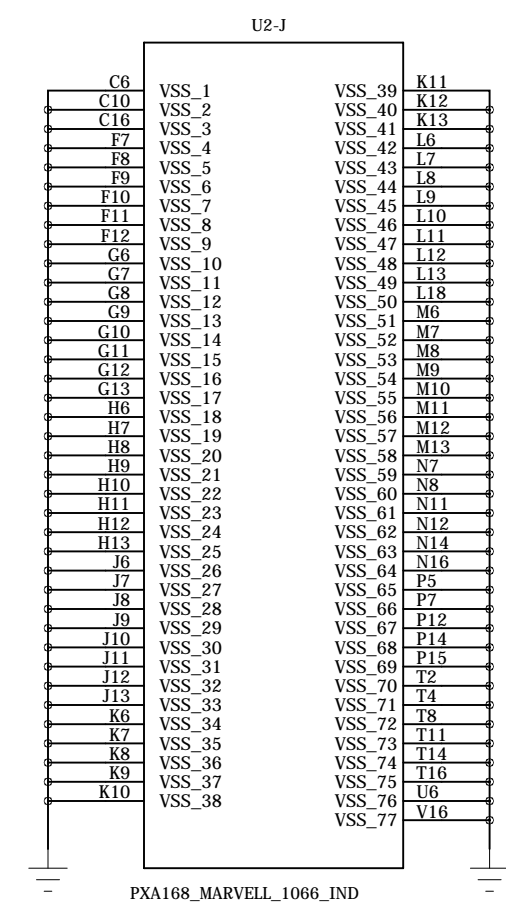


PXA168 PCIe rails must be connected to AN_1.8V

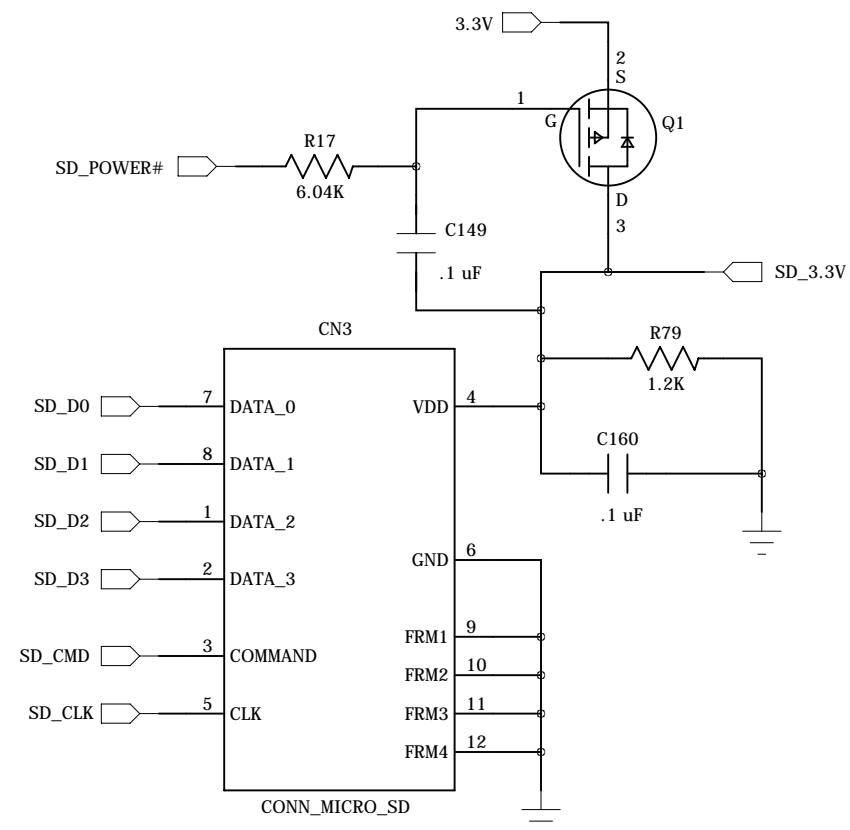


CPU

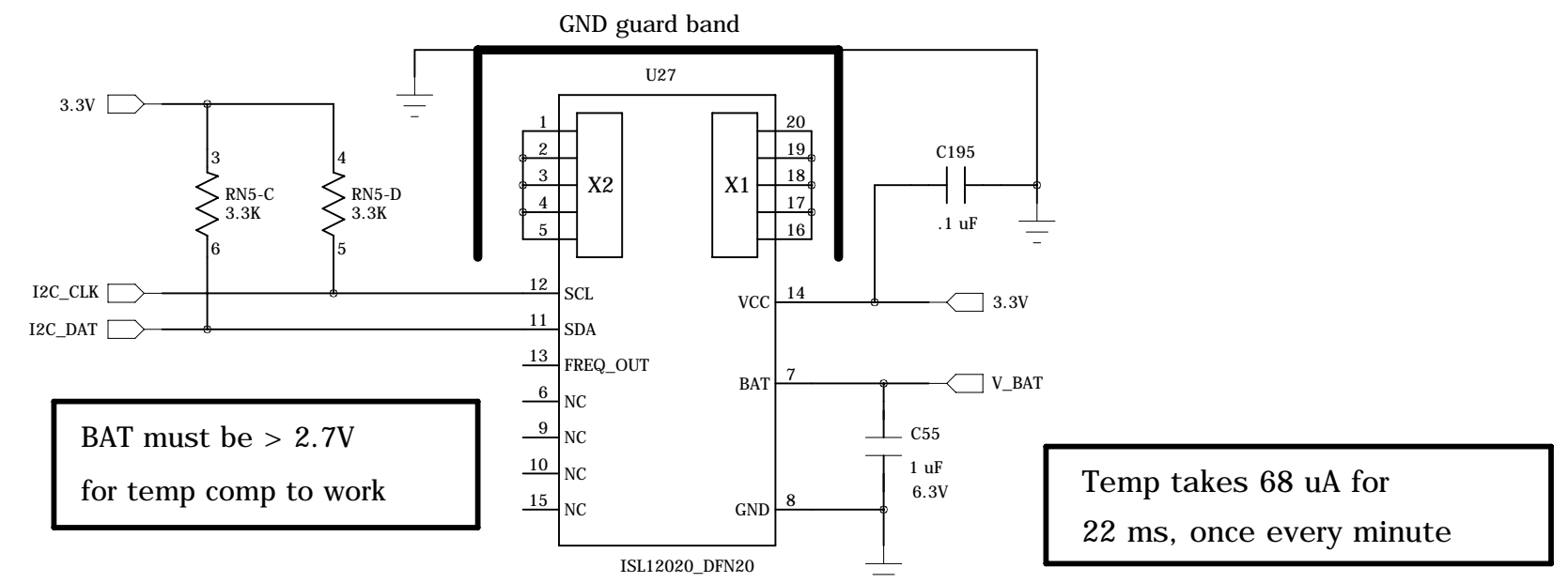
CPU



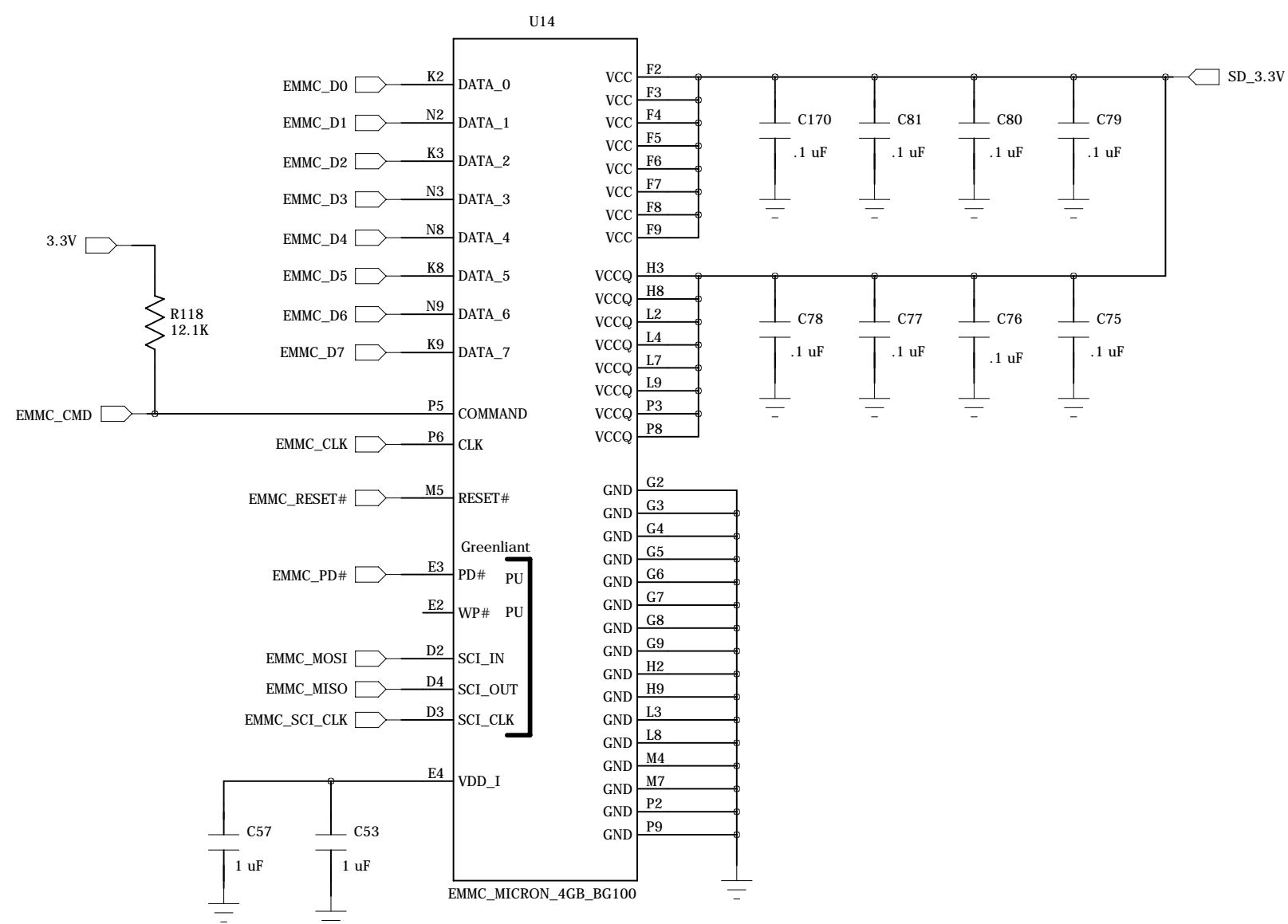
Micro SD Card Socket



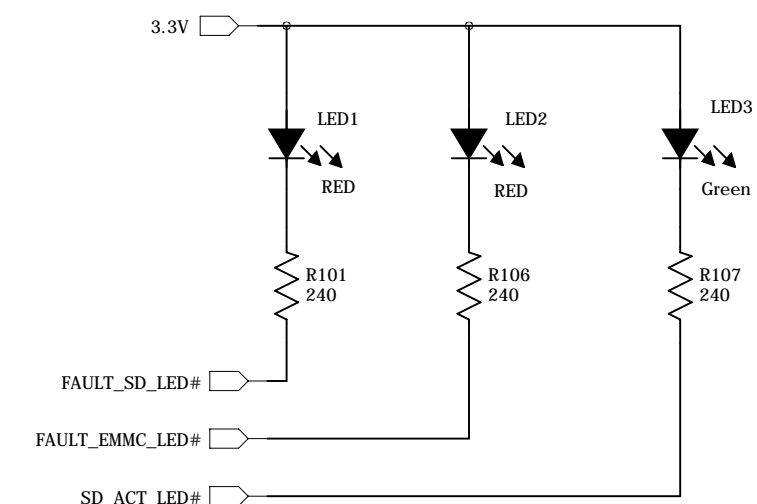
RTC and Temp. Sensor



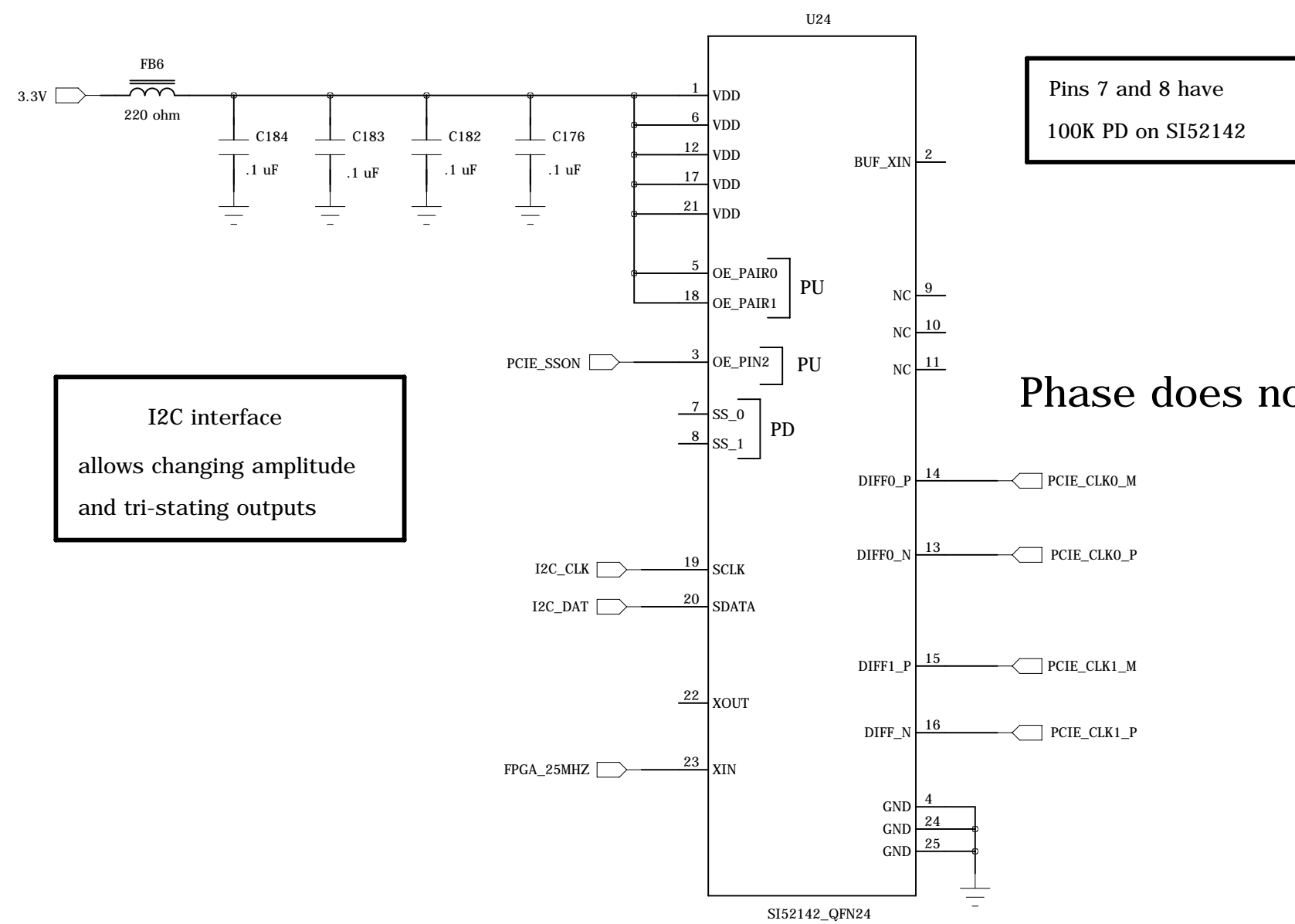
eMMC 4GB



SD Card LEDs



PCIe 100 MHz Clock Generator



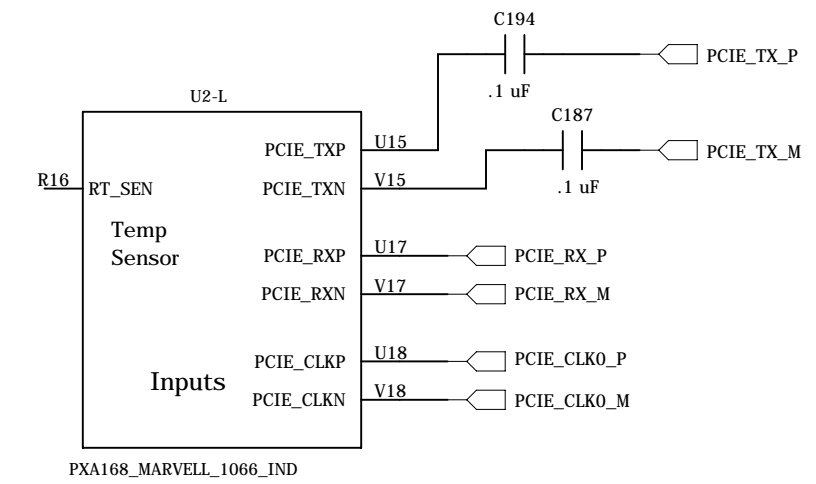
Pins 7 and 8 have
100K PD on SI52142

I2C interface
allows changing amplitude
and tri-stating outputs

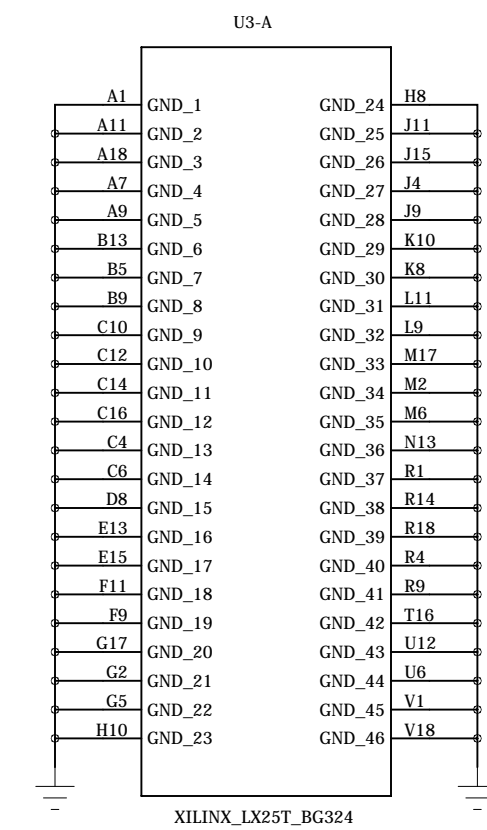
Phase does not matter

CPU PCIe

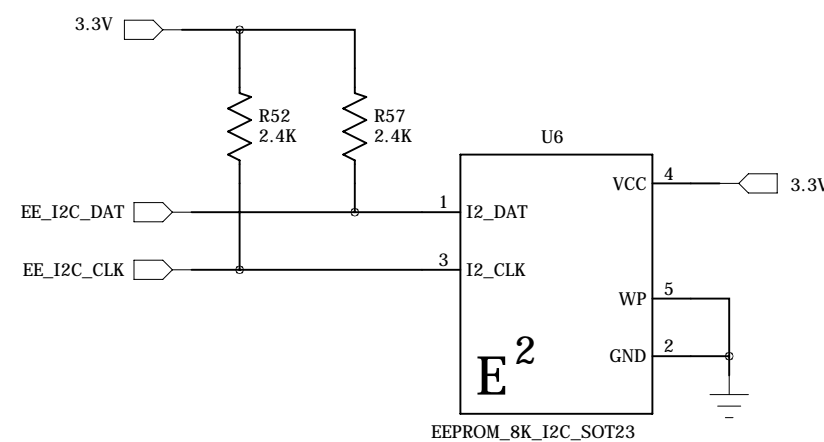
PCIe not supported
on PXA166



FPGA GND

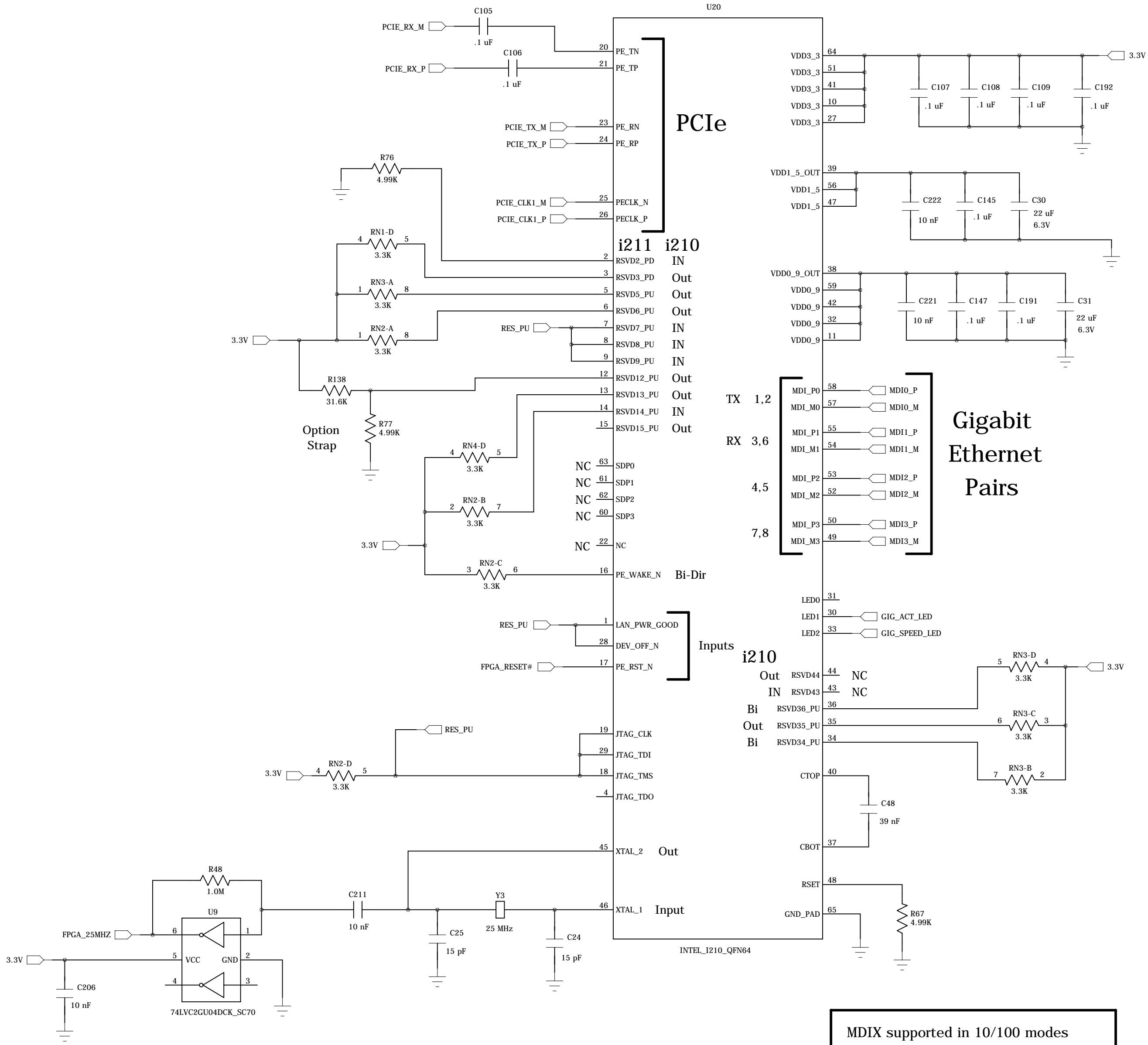


EEPROM 1 Kbyte



I2C address is same as RTC !

Gigabit Ethernet Controller



MDIX supported in 10/100 modes

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 600 mA

EXT_RESET# is an Input
used to reboot the CPU

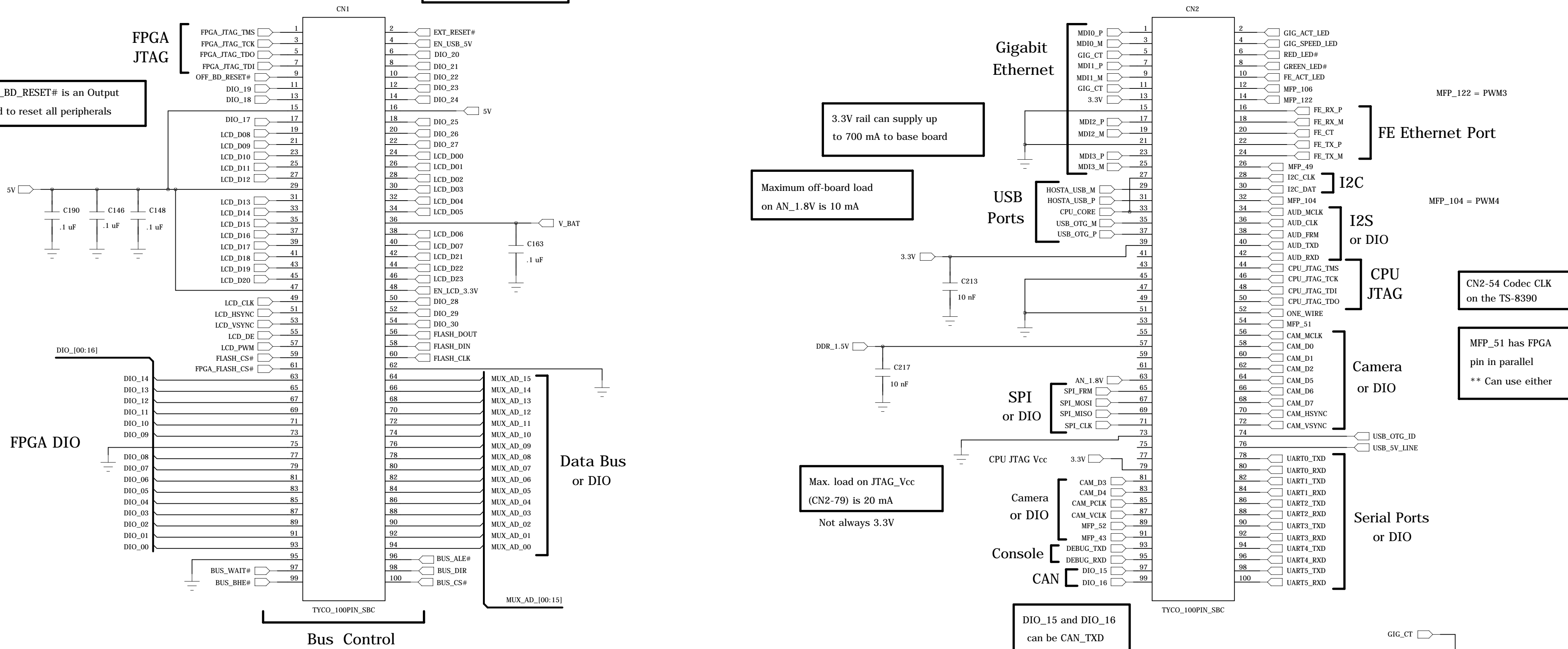
Do not drive active high
(use open drain)

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

OFF_BD_RESET# is an Output
used to reset all peripherals

Left

Right



3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on AN_1.8V is 10 mA

Max. load on JTAG_Vcc
(CN2-79) is 20 mA
Not always 3.3V

DIO_15 and DIO_16
can be CAN_TXD
and CAN_RXD

If Bus is not needed, all Bus
signals can be changed to DIO

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

CN2-54 Codec CLK
on the TS-8390

MFP_51 has FPGA
pin in parallel
** Can use either