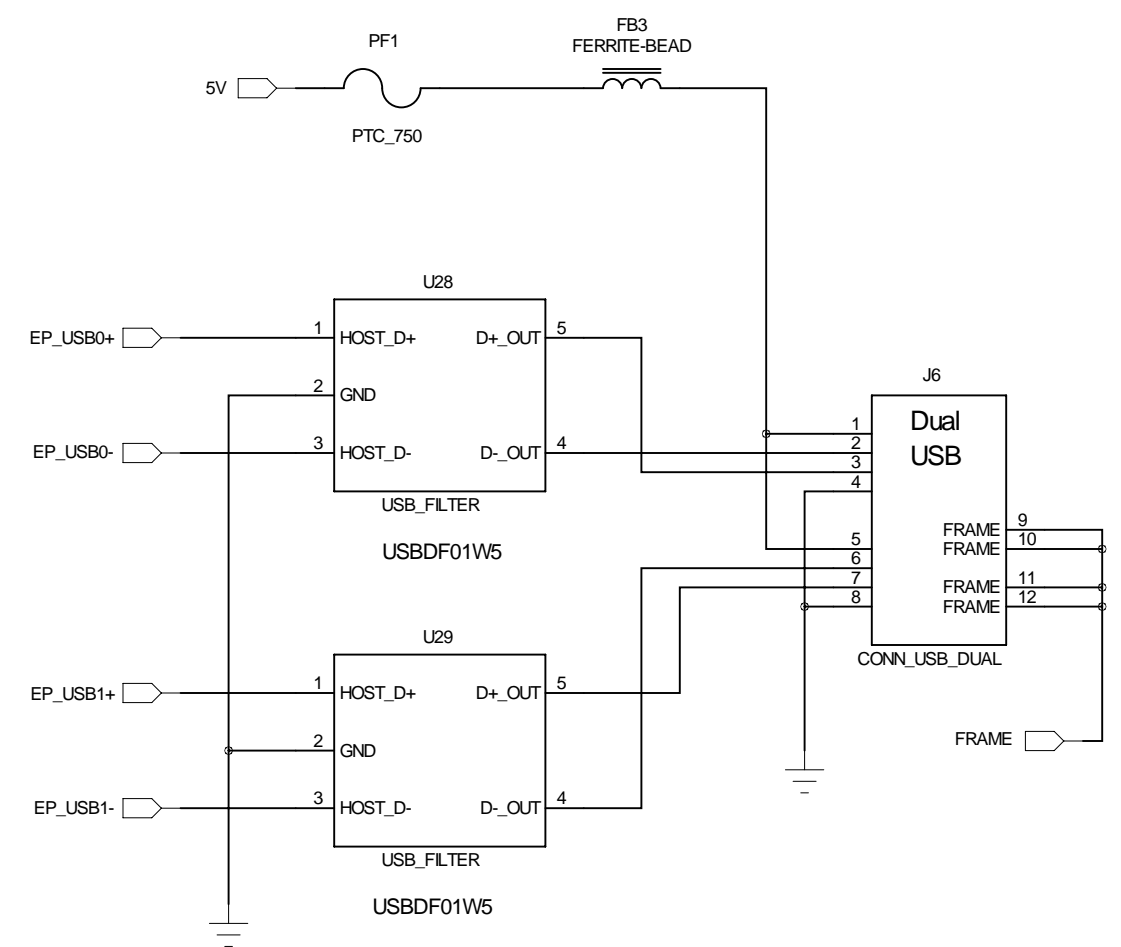
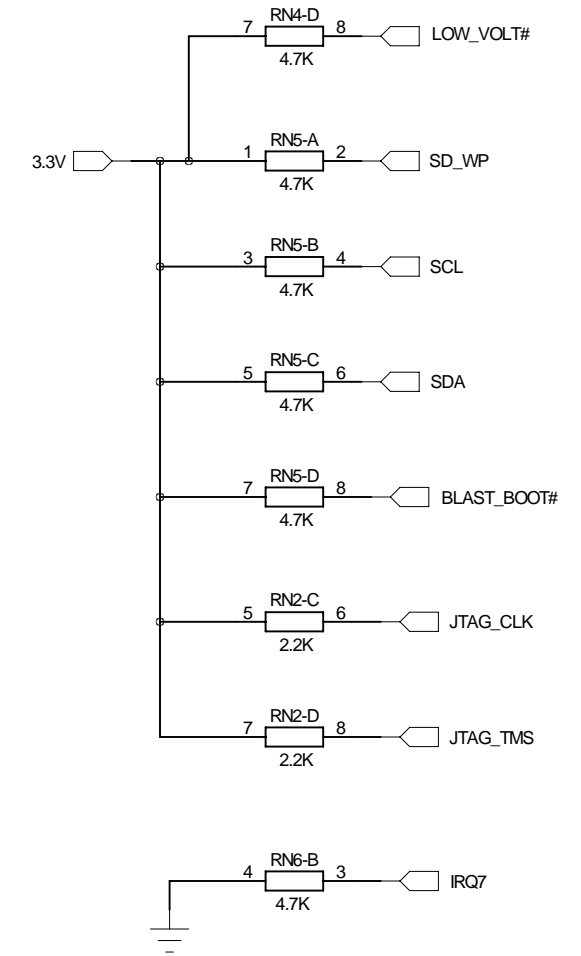
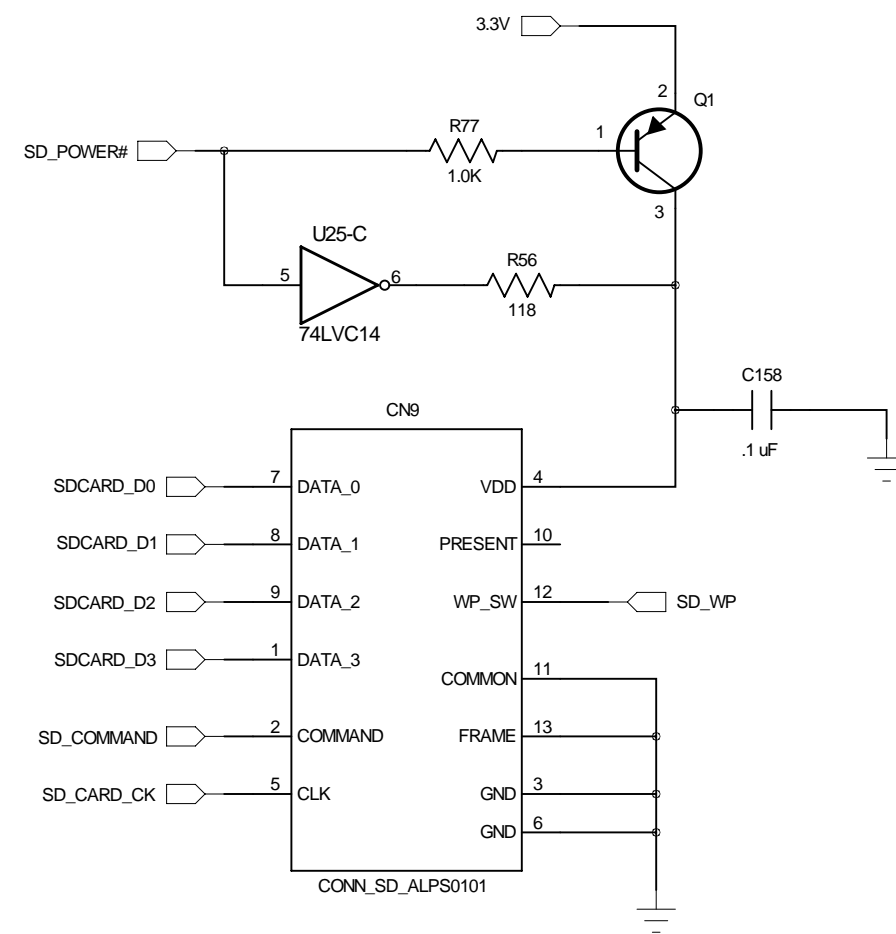


USB Ports

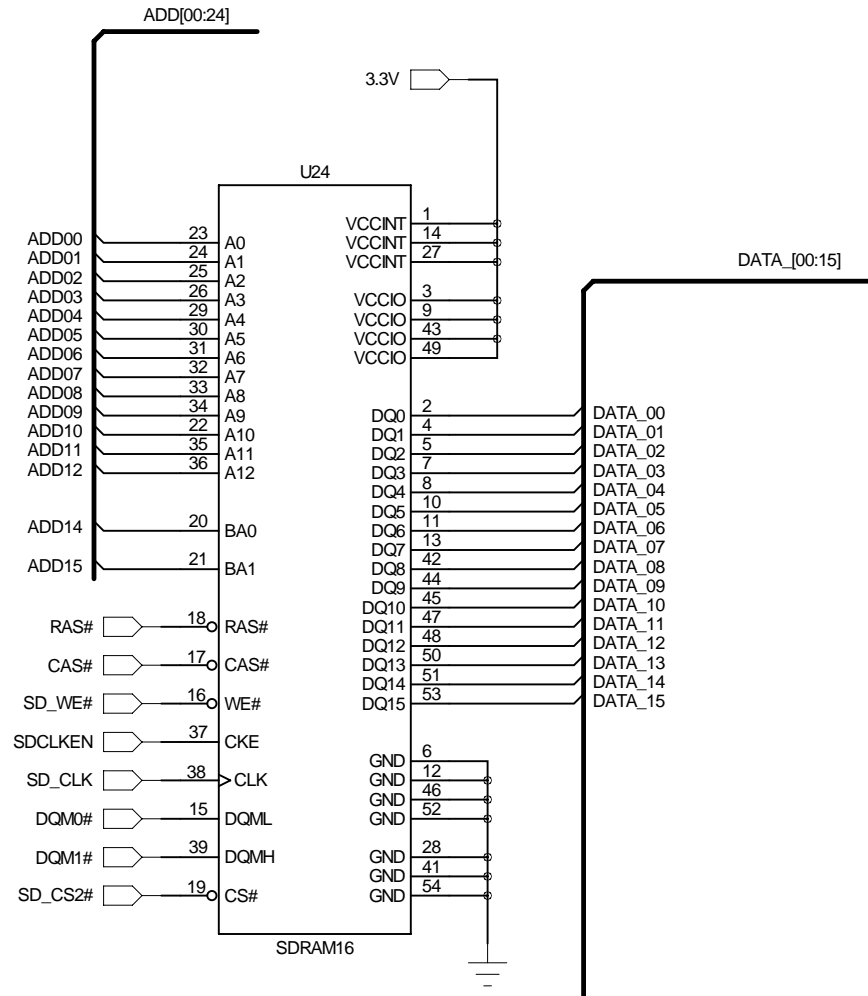


Technologic Systems		Date	Oct. 7, 2008
Title: TS-7390 EP9302 CPU, USB			
Rev.	Designer	RLM	Sheet 1 of 8

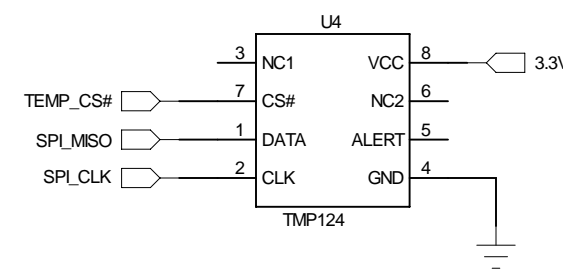
SD Card Socket



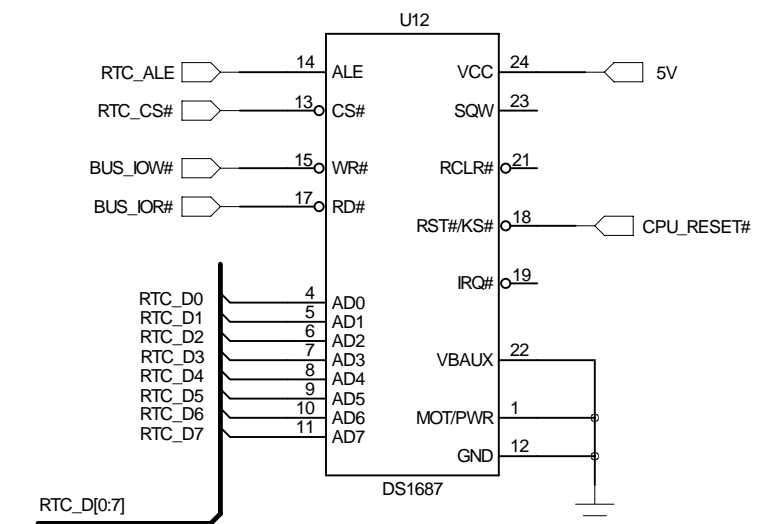
SDRAM



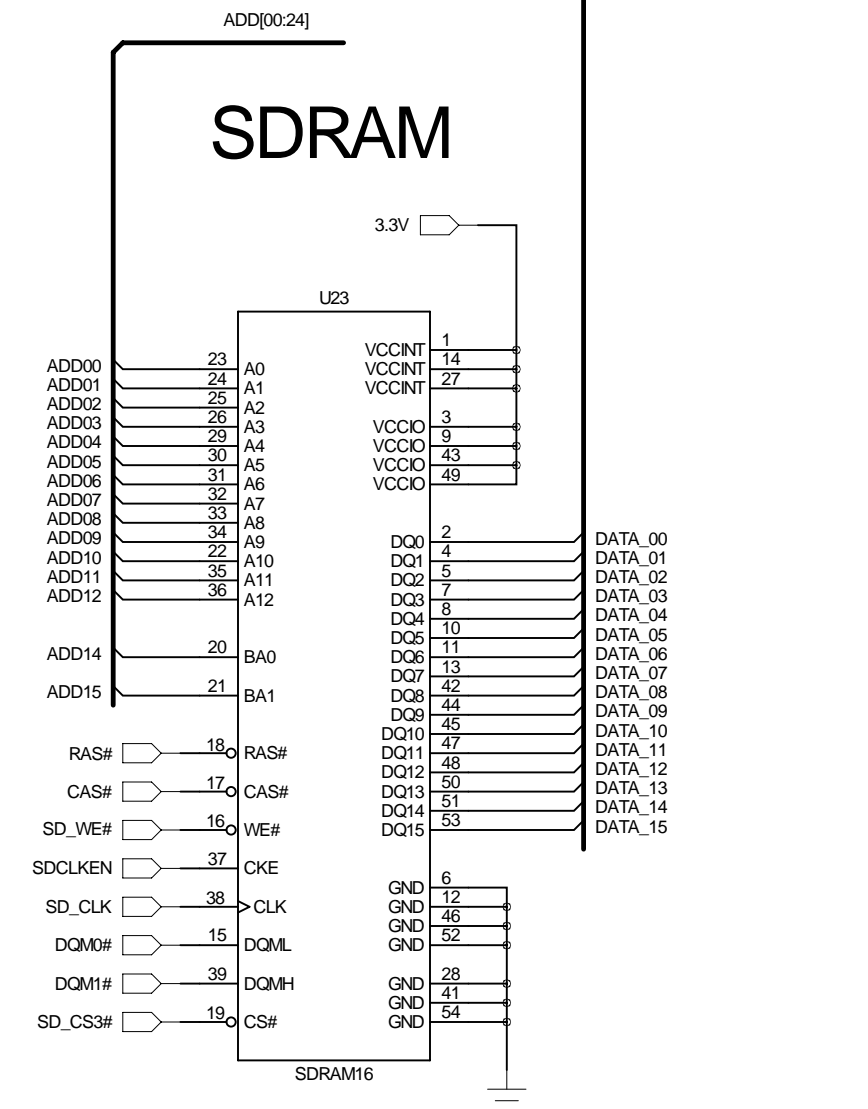
Temp Sensor



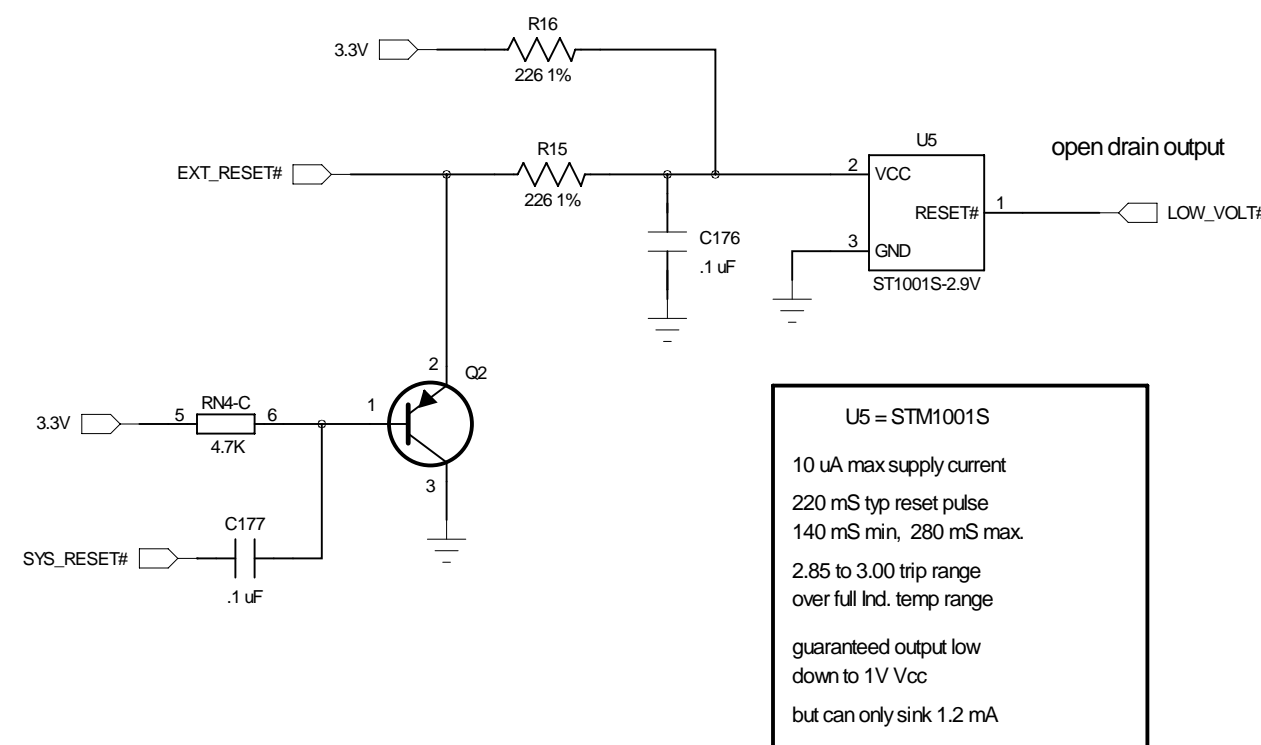
Battery-Backed Real Time Clock



SDRAM

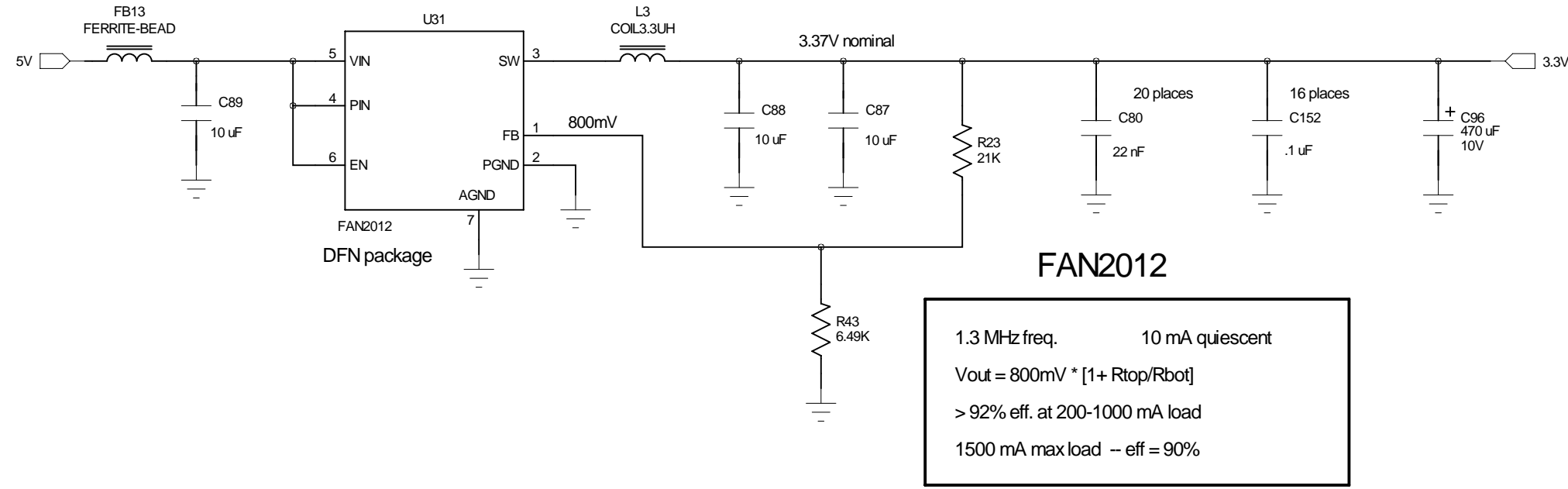


Power On Reset



Technologic Systems	Date	Oct. 7, 2008
Title:	TS-7390 SDRAM, Flash, RTC, POR	
Rev:	Designer	RLM
	Sheet	2 of 8

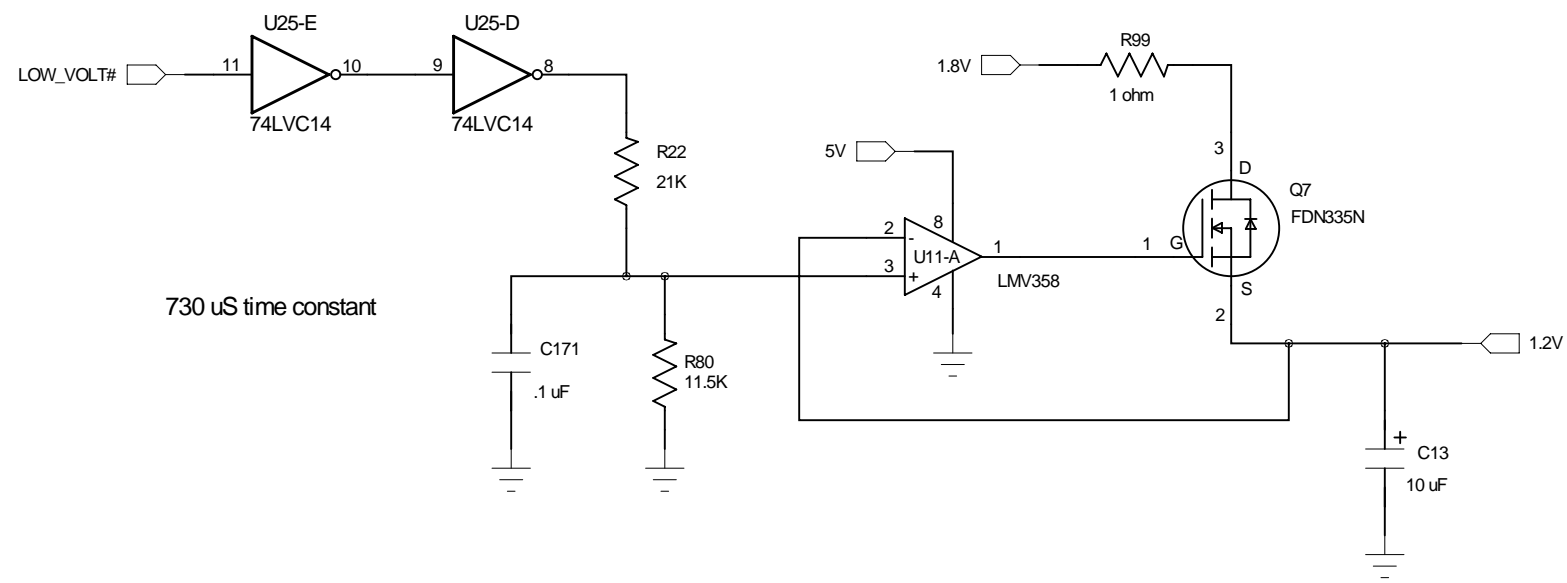
3.3V Switching Regulator



FAN2012

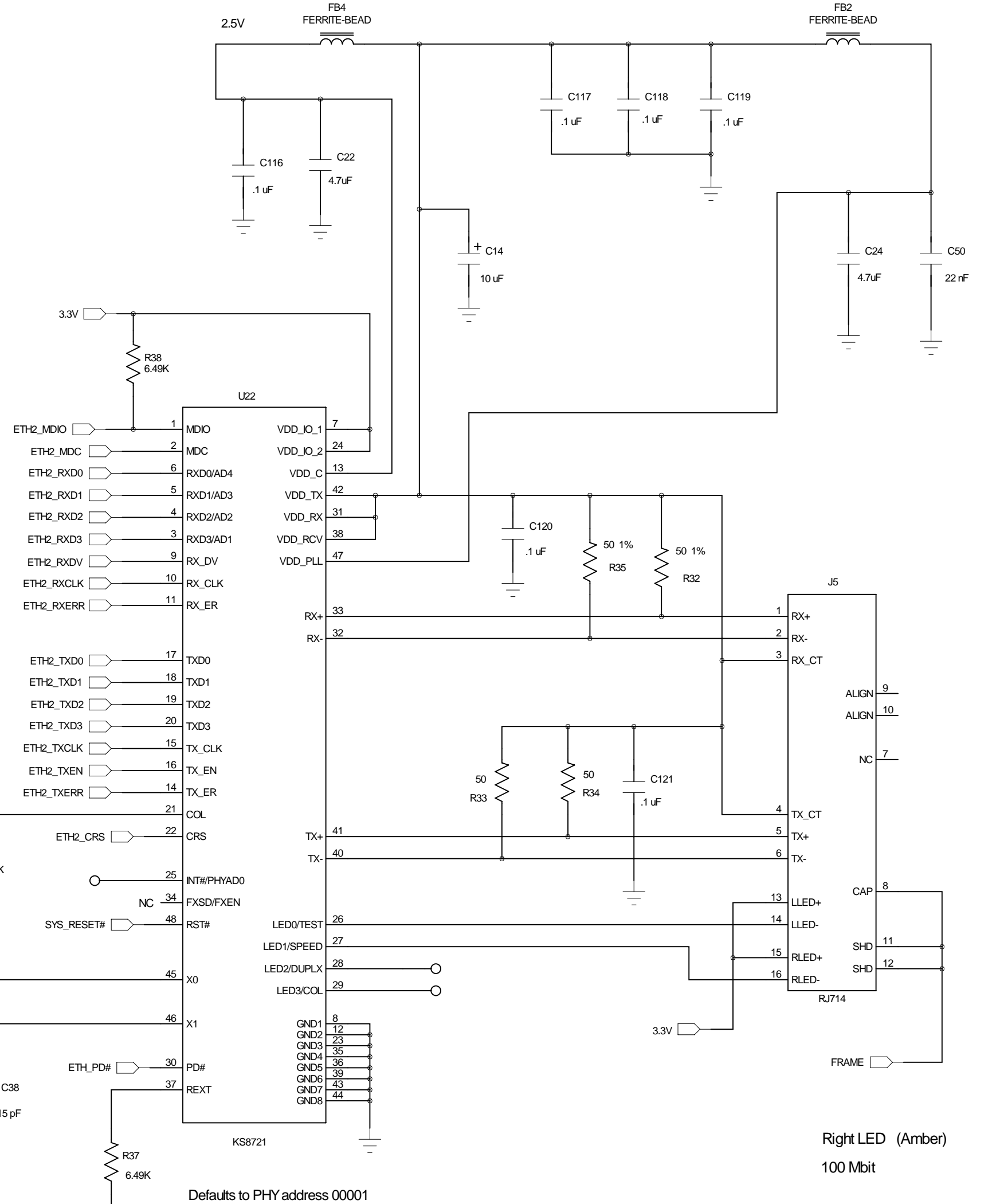
1.3 MHz freq. 10 mA quiescent
 $V_{out} = 800mV * [1 + R_{top}/R_{bot}]$
 > 92% eff. at 200-1000 mA load
 1500 mA max load -- eff = 90%

1.2V Regulator



730 µs time constant

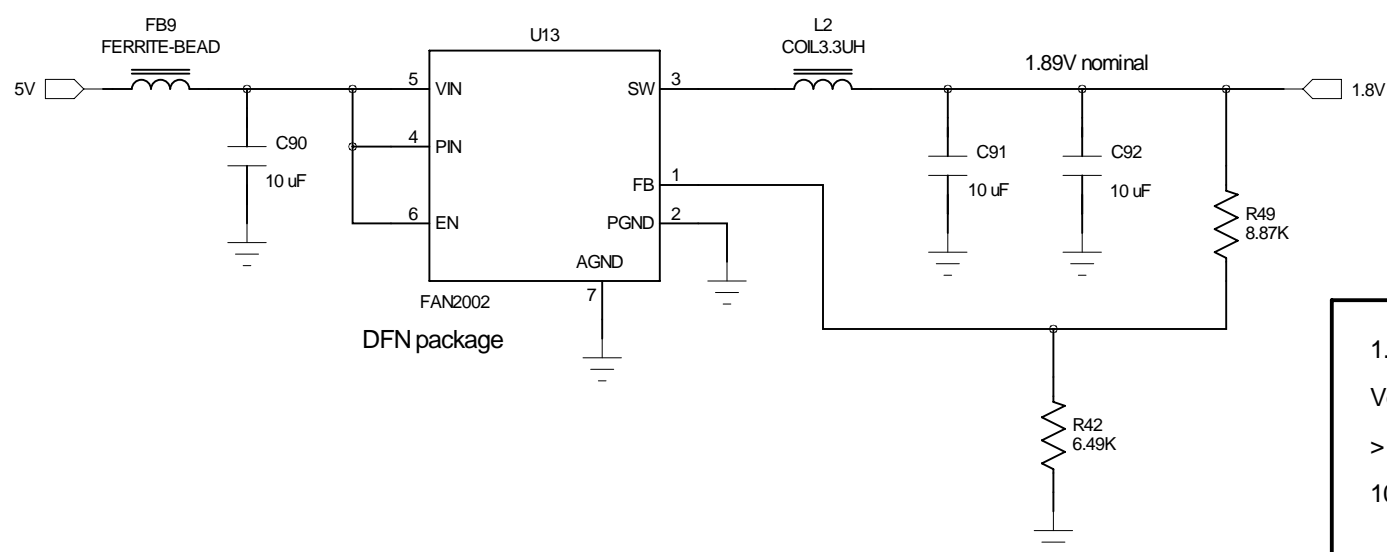
10/100 Ethernet



Right LED (Amber)
100 Mbit

Left LED (Green)
Link / Activity

1.8V Switching Regulator

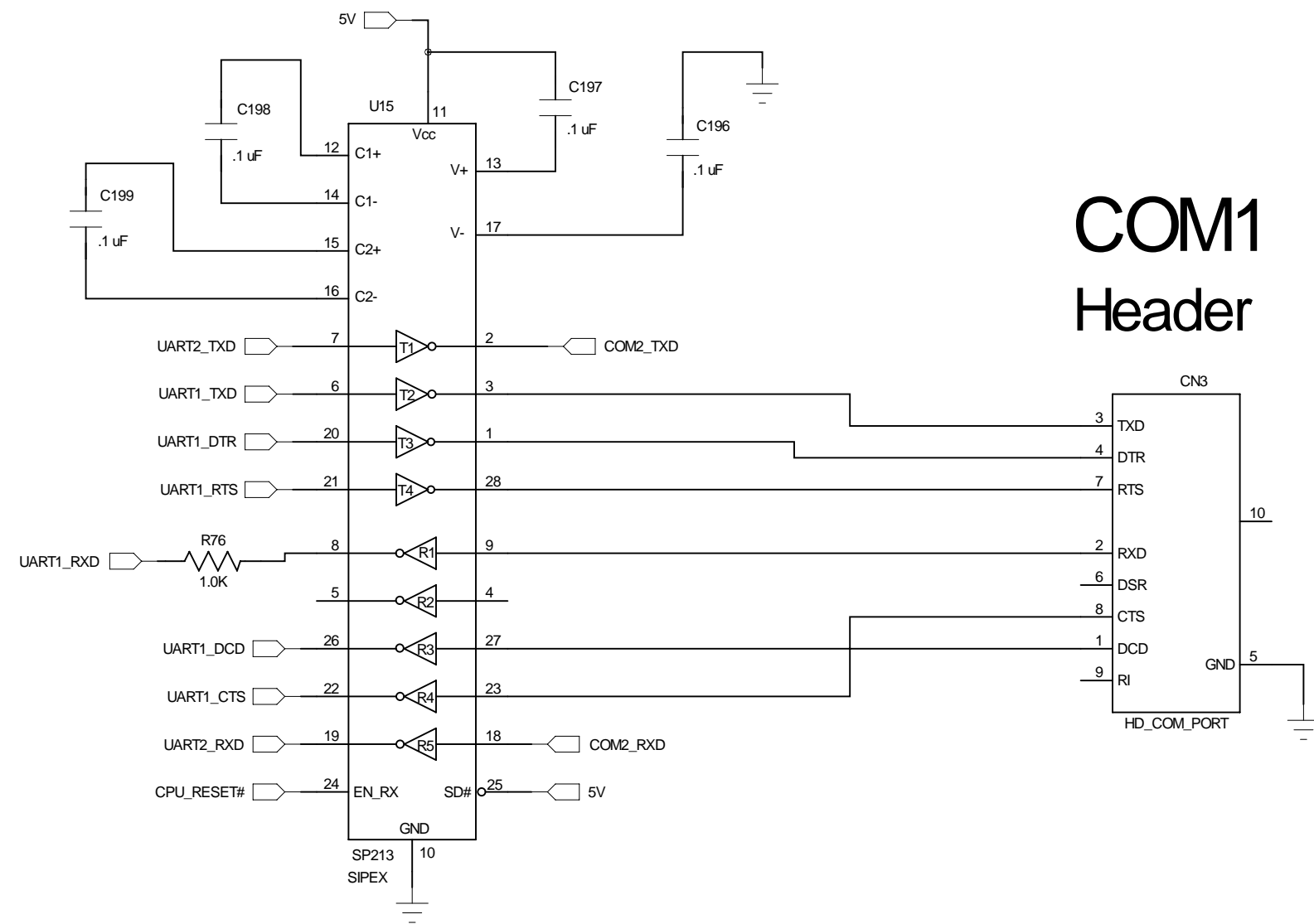


FAN2002

1.3 MHz freq. 50 µA quiescent
 $V_{out} = 800mV * [1 + R_{top}/R_{bot}]$
 > 90% eff. at 100-400 mA load
 1000 mA max load; eff. = 80%
 (at 5V -> 1.8V)

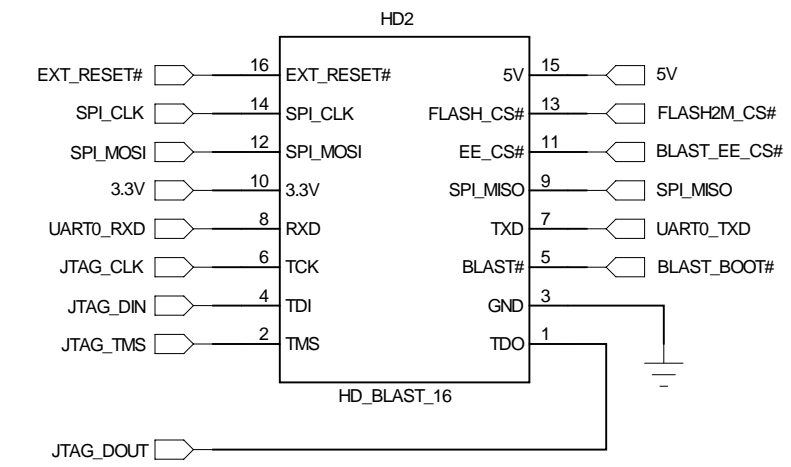
Technologic Systems	Date	Oct. 7, 2008
Title: TS-7390 Power Supplies, Ethernet		
Rev.	Designer	RLM
Sheet		3 of 8

RS-232 Transceiver



COM1 Header

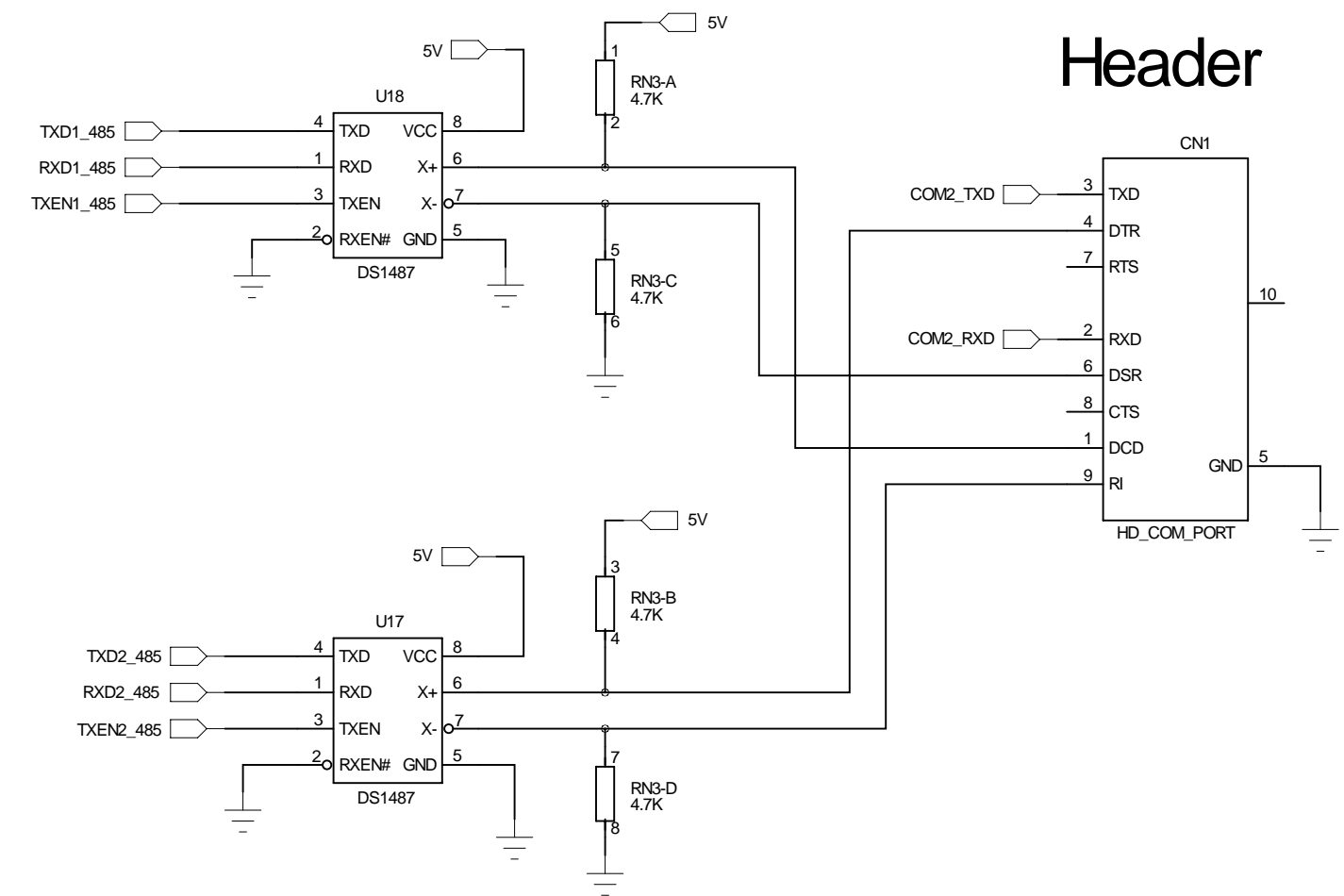
JTAG Header



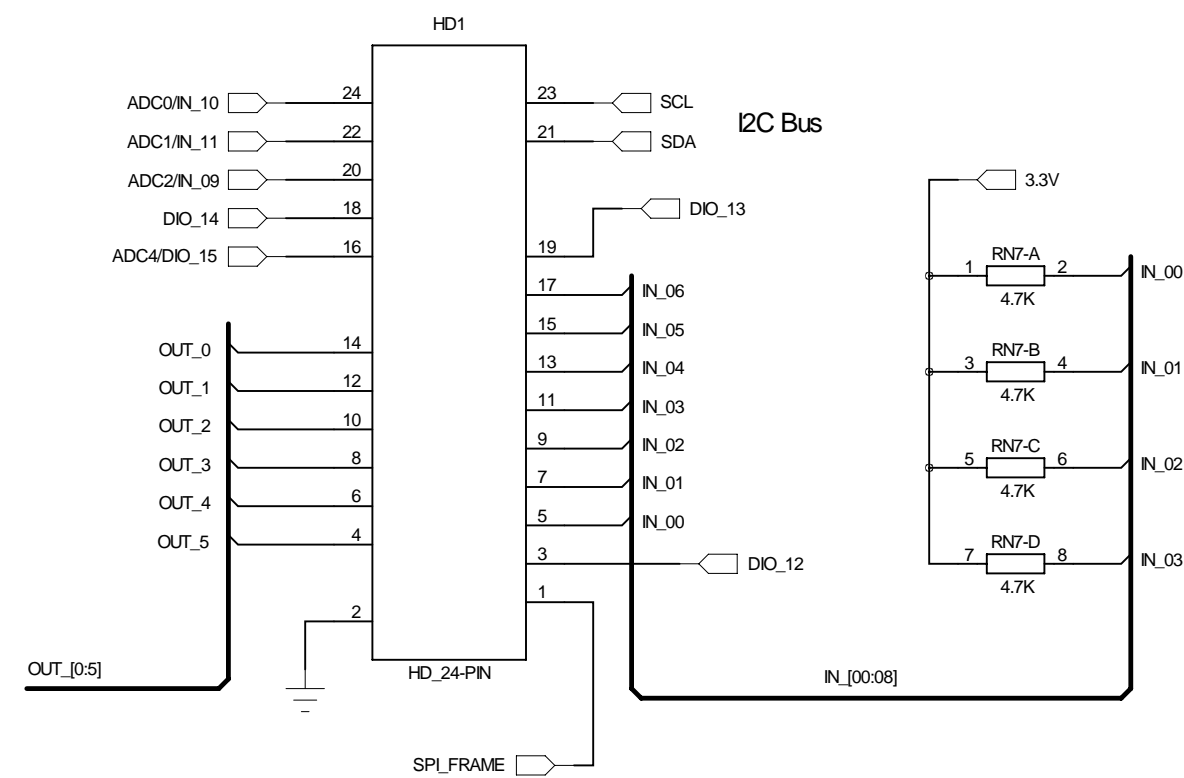
BLAST_EE_CS# is not used for booting -- FPGA Boot code has capability to boot from 2MB Serial Flash directly

Logic "0" on "BLAST_BOOT#" signal indicates Boot using TS-9444 2MB Flash

RS-485 Drivers



COM2 Header



24-pin Header

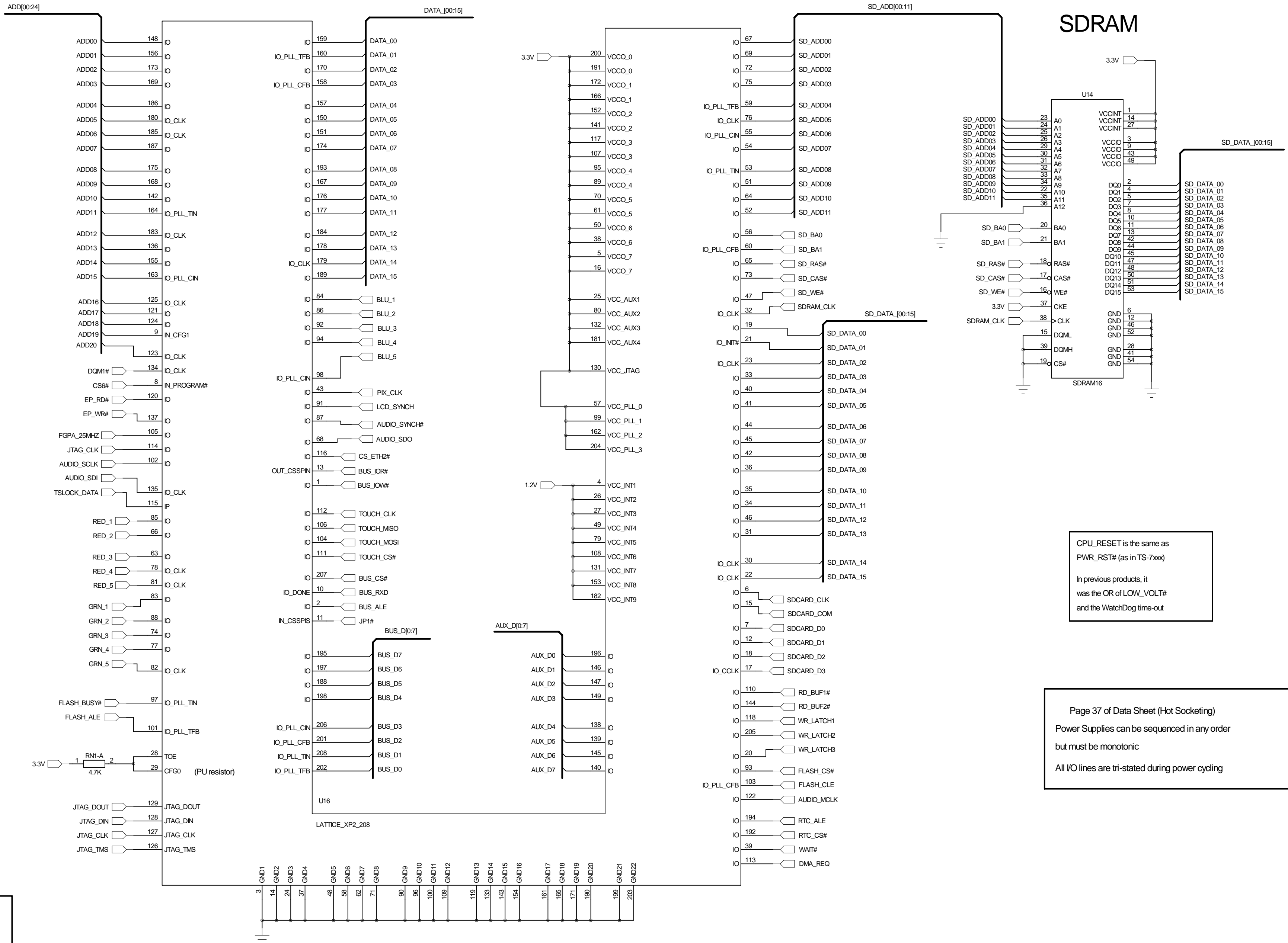
24 + 16 = 40-pin Header

- 4 ADC
ADC lines in parallel with IN_09, IN_10, IN11, DIO15
- 2 I2C
- 1 GND
- 6 Latched Outputs (OUT0-OUT5)
- 7 Buffered Inputs (IN0-IN6)
- 3 DIO_12, DIO_13, DIO_14
- 1 SPL_FRAME

Technologic Systems	Date	Oct. 7, 2008
Title:	TS-7390 COM Ports DIO JTAG Headers	
Rev:	Designer	Sheet 4 of 8

Lattice XP2 FPGA

8 MB Video SDRAM



XP2-5 has:
 5K LUTS 2 PLLs
 9 blocks of 1Kx18 Block RAM
 12 18x18 Multipliers
 146 I/O with 208 pin package
 "instant ON" = about 1.5 mS
 input PLL clock = 10 MHz min

Make sure these signals are on CLK inputs:
 SDRAM_CLK
 FPGA_25MHz

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"
 Page 4 of TN1141

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash -> SRAM
 DONE likewise must be high
 These do have weak PU resistors

Pins 28 and 29 must be pulled up! 3.3V suggested

When CFG0 = 1 then always uses SDM
 SDM = Self Download Mode
 SDM uses on-chip Flash -> SRAM
 CFG0 PU resistor uses VCC core (1.2V)

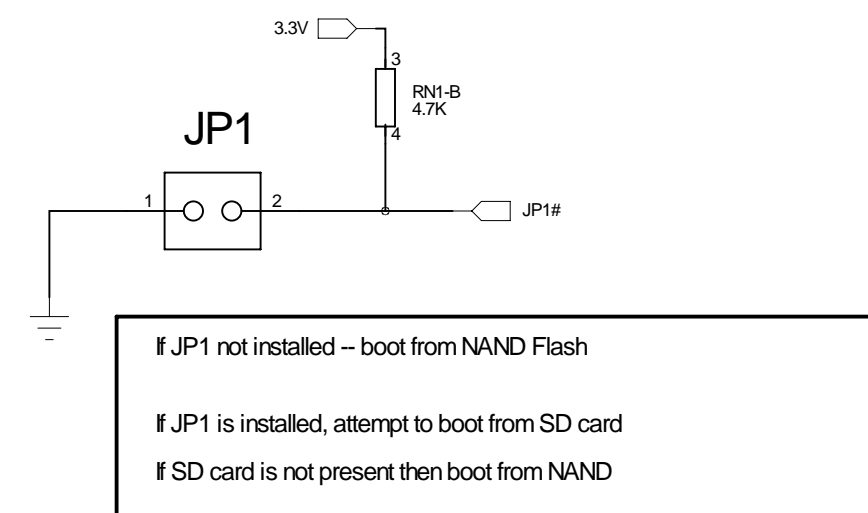
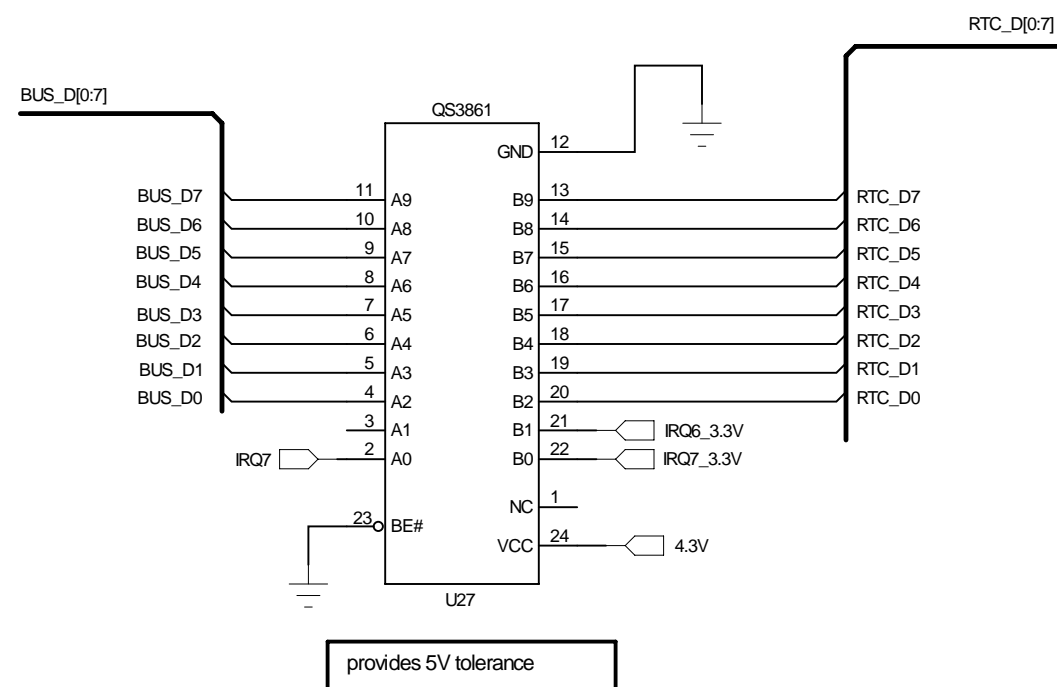
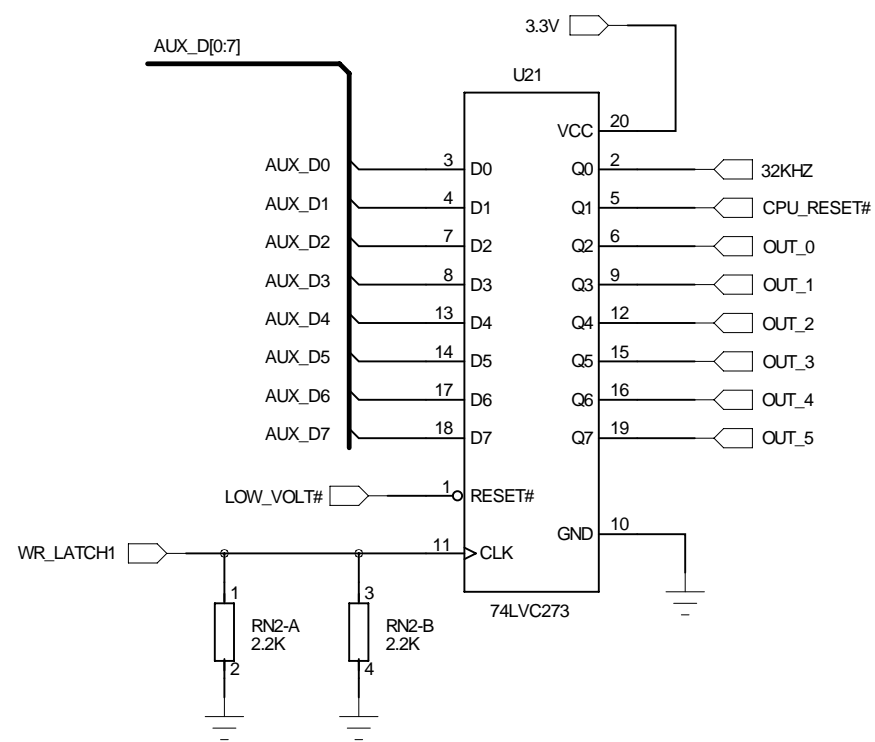
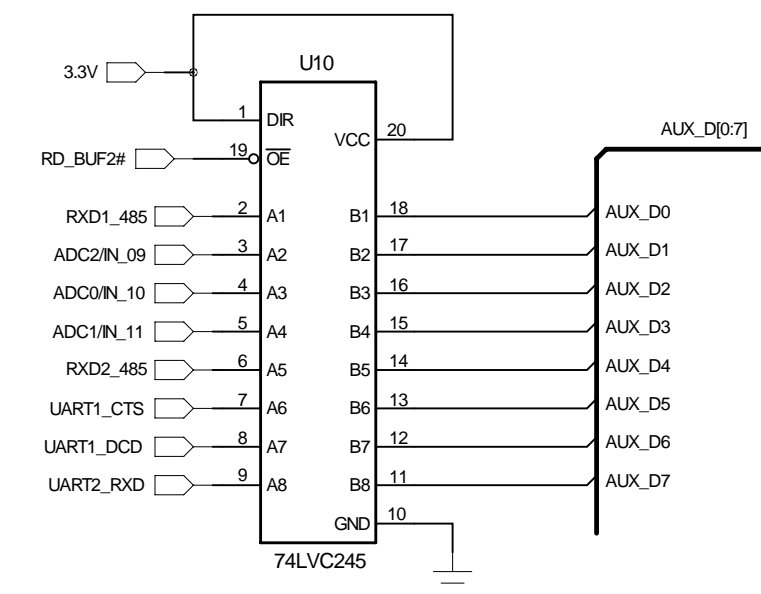
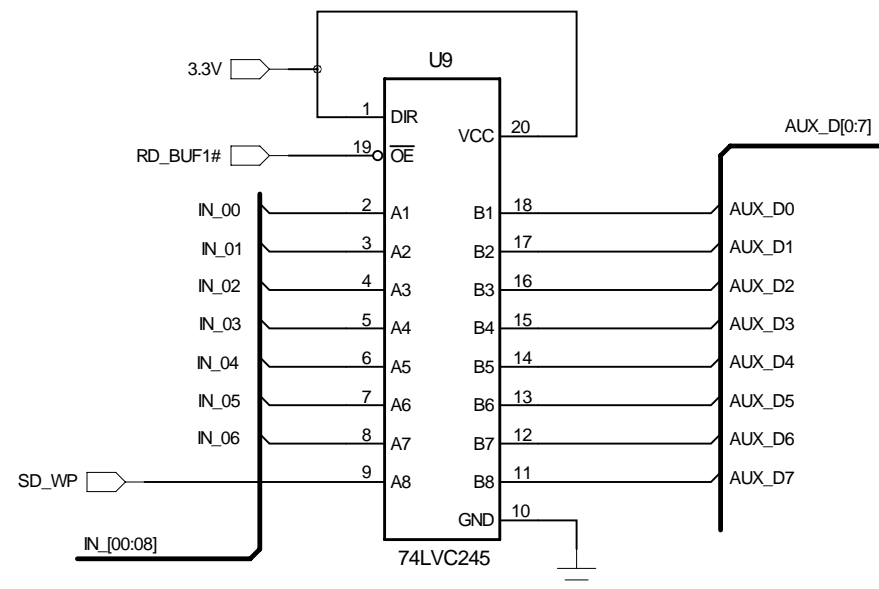
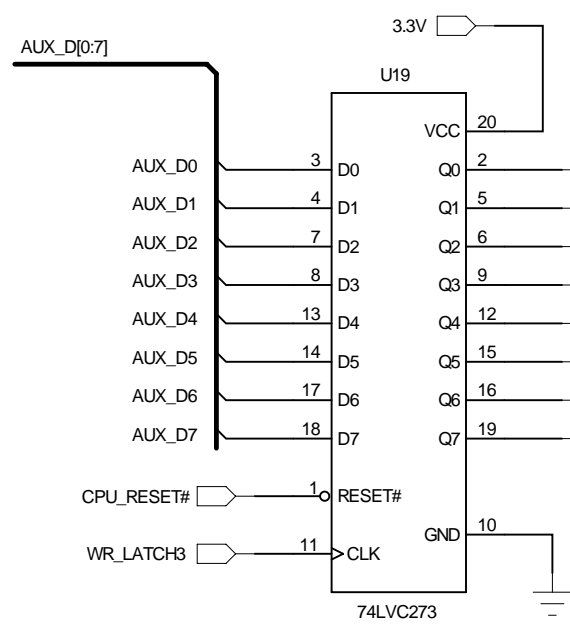
TAG Memory is 79 bytes of Flash (XP2-5)
 Always available thru JTAG port
 can not be Write or Read protected
 perfect for: MAC, birth date, Revision#
 TAG memory can be accessed from fabric

Set CONFIG_MODE to NONE
 This allows all pins to be used

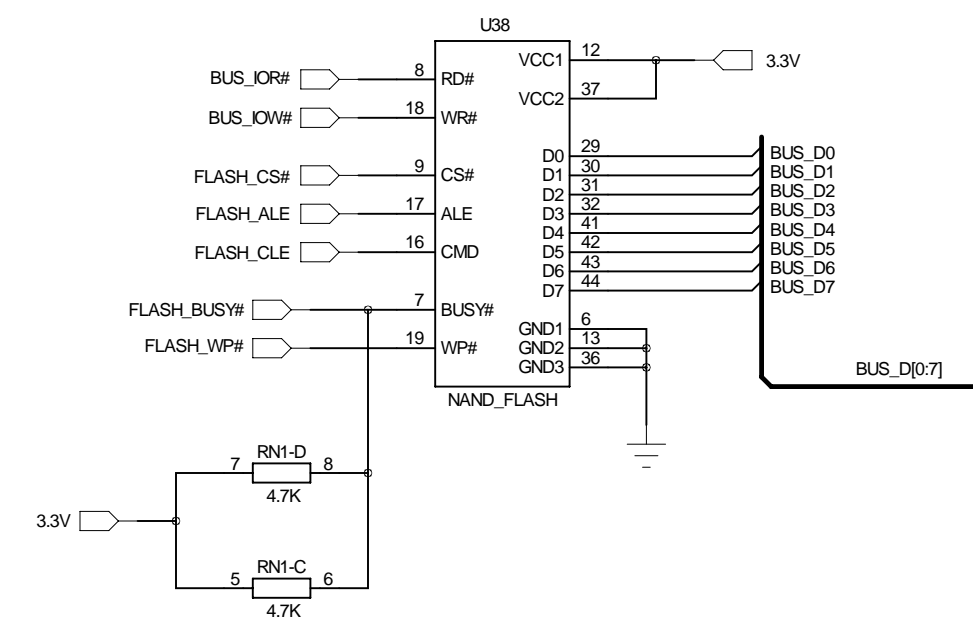
Pull-up and pull-down resistors are 6 to 30K ohms

CPU_RESET is the same as PWR_RST# (as in TS-7xxx)
 In previous products, it was the OR of LOW_VOLT# and the WatchDog time-out

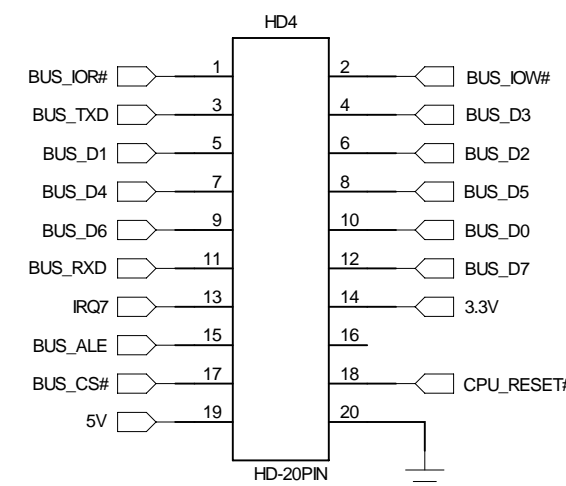
Page 37 of Data Sheet (Hot Socketing)
 Power Supplies can be sequenced in any order but must be monotonic
 All I/O lines are tri-stated during power cycling



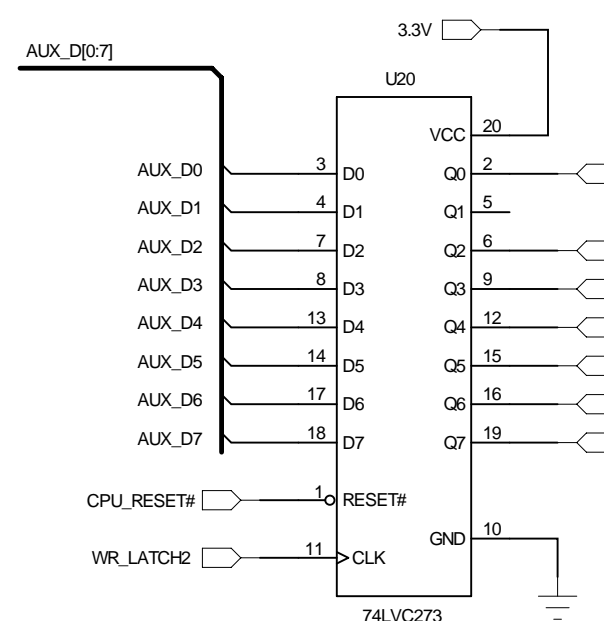
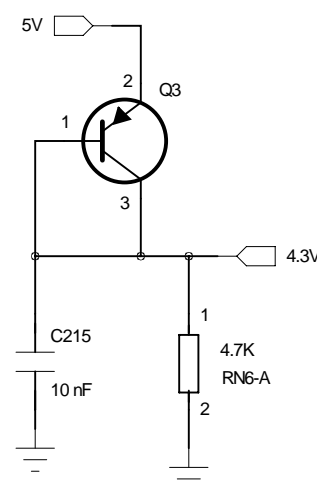
NAND Flash



Expansion Bus



4.3V Power Supply



EN_LCD_3.3V is removed on Rev B board

Technologic Systems		Date	Oct. 7, 2008
Title:	TS-7390 AUX Bus		
Rev.	Designer	Sheet	6 of 8

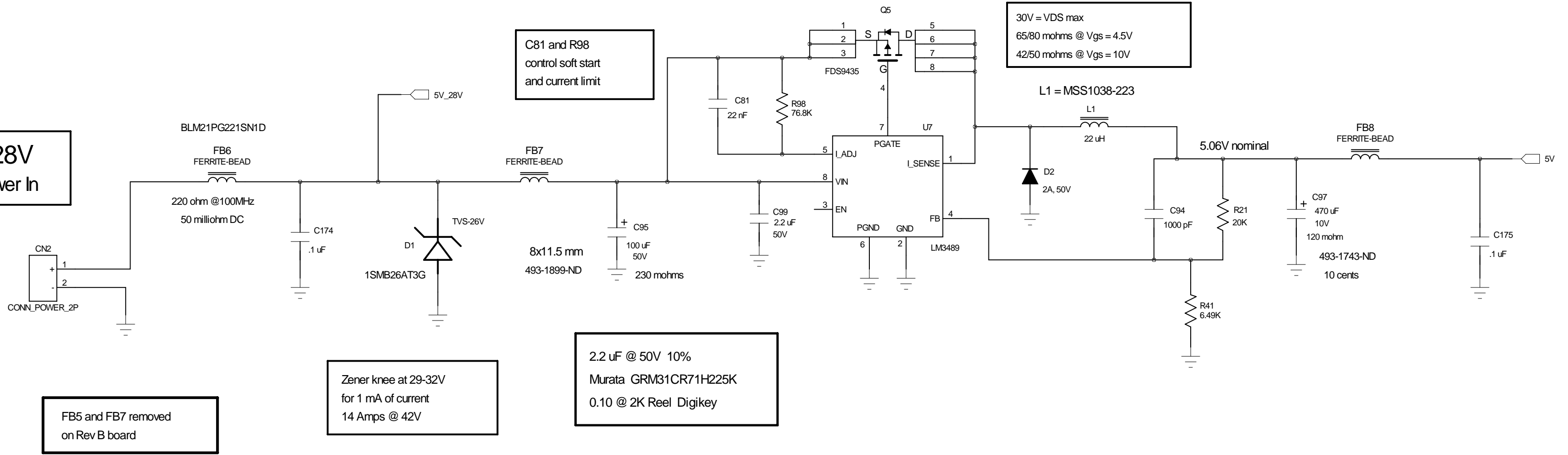
Hysteretic Switching Power Supply

5V @ (2.5 Amps)

5-28V
Power In

C81 and R98
control soft start
and current limit

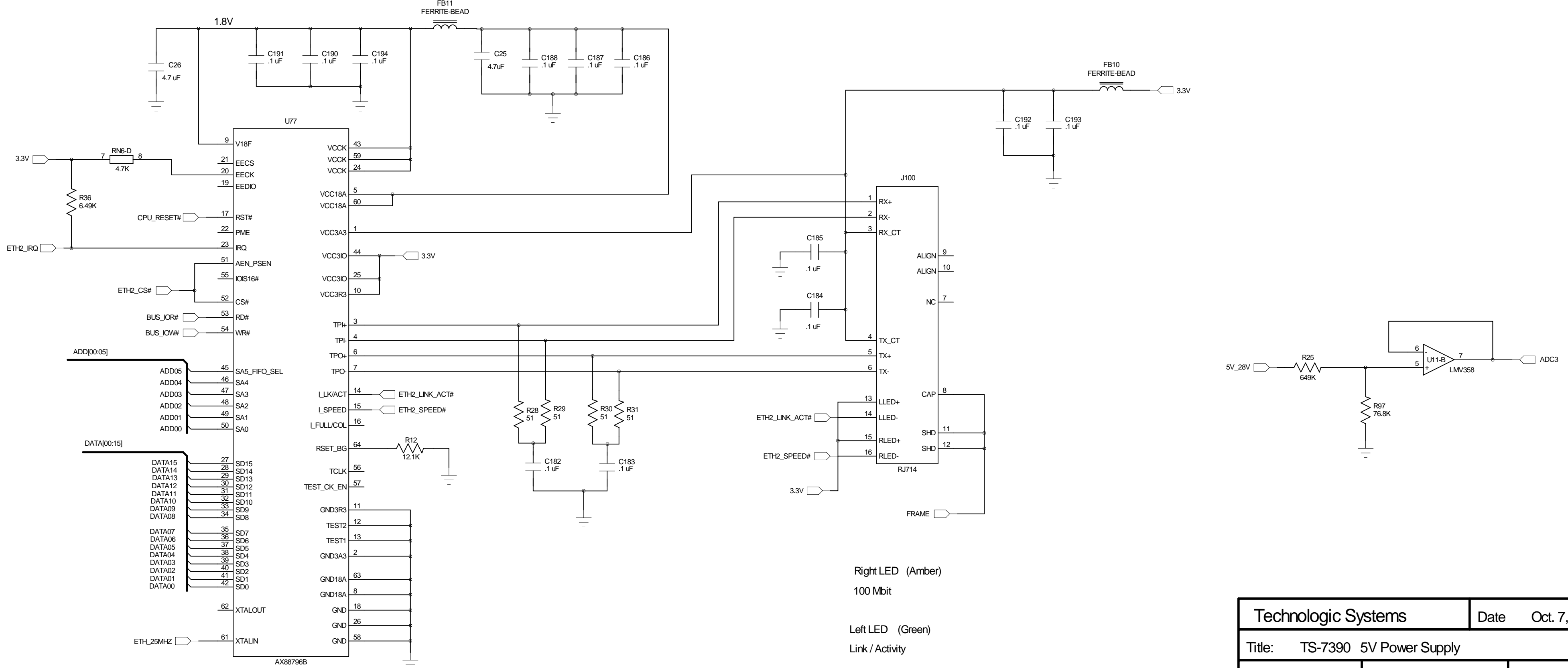
30V = VDS max
65/80 mohms @ Vgs = 4.5V
42/50 mohms @ Vgs = 10V



FB5 and FB7 removed
on Rev B board

Zener knee at 29-32V
for 1 mA of current
14 Amps @ 42V

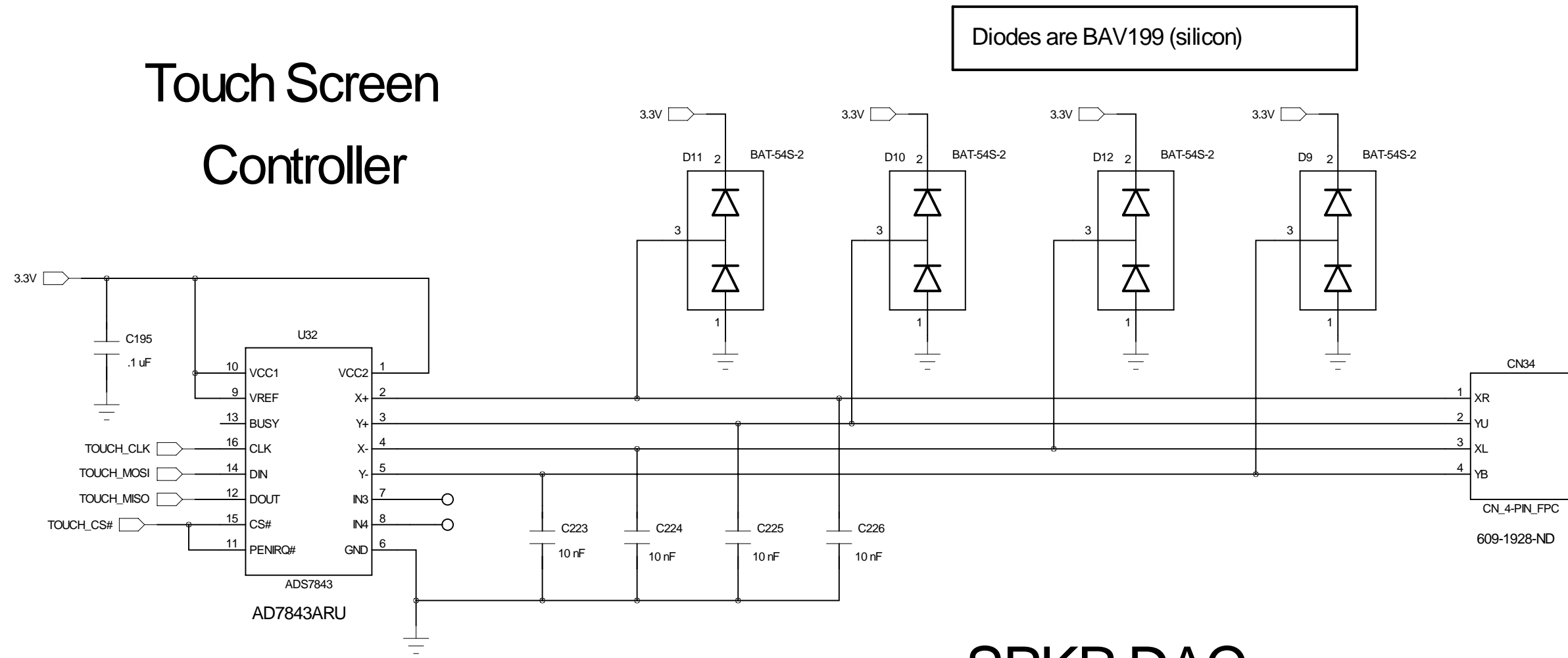
2.2 uF @ 50V 10%
Murata GRM31CR71H225K
0.10 @ 2K Reel Digikey



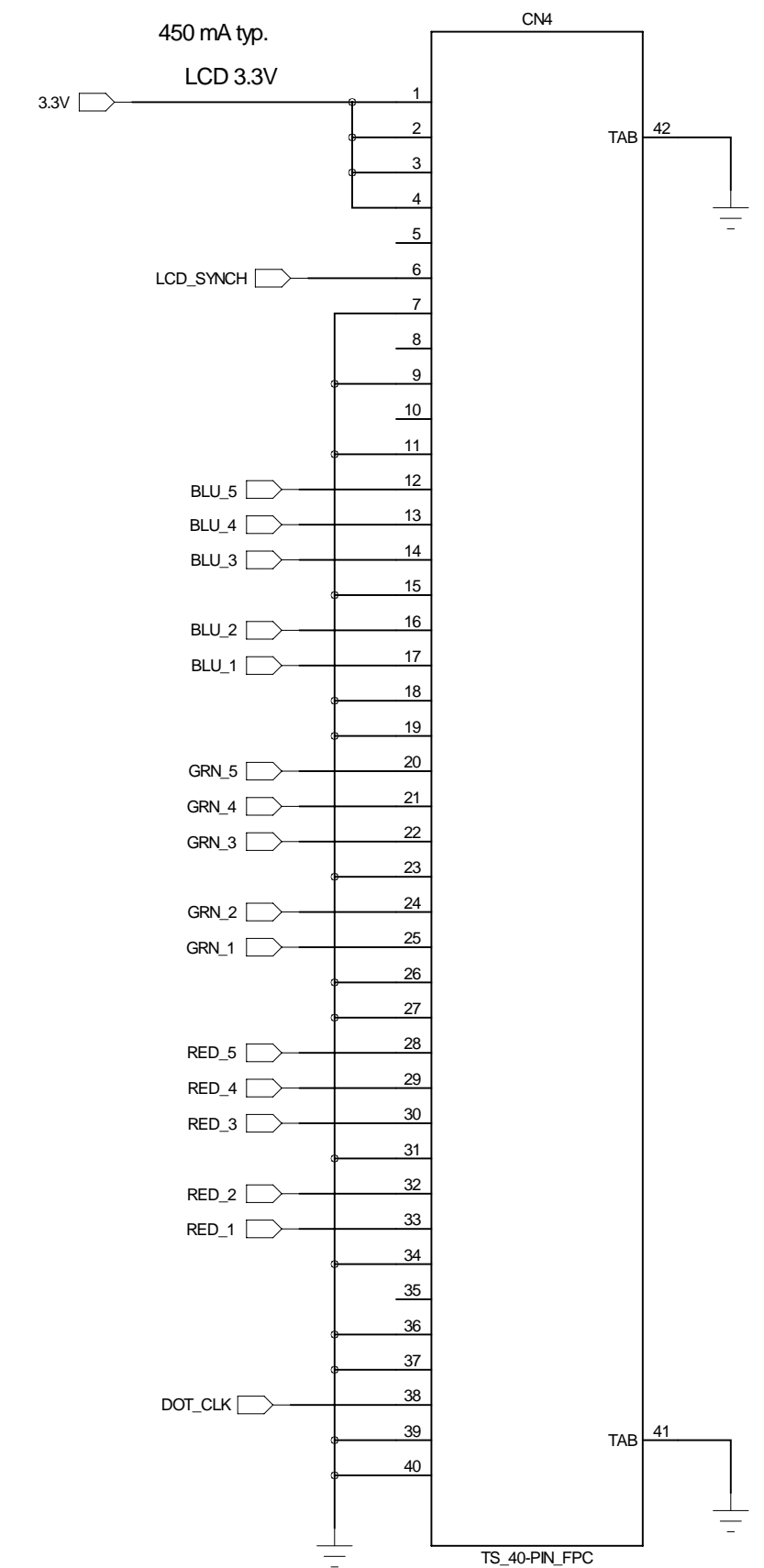
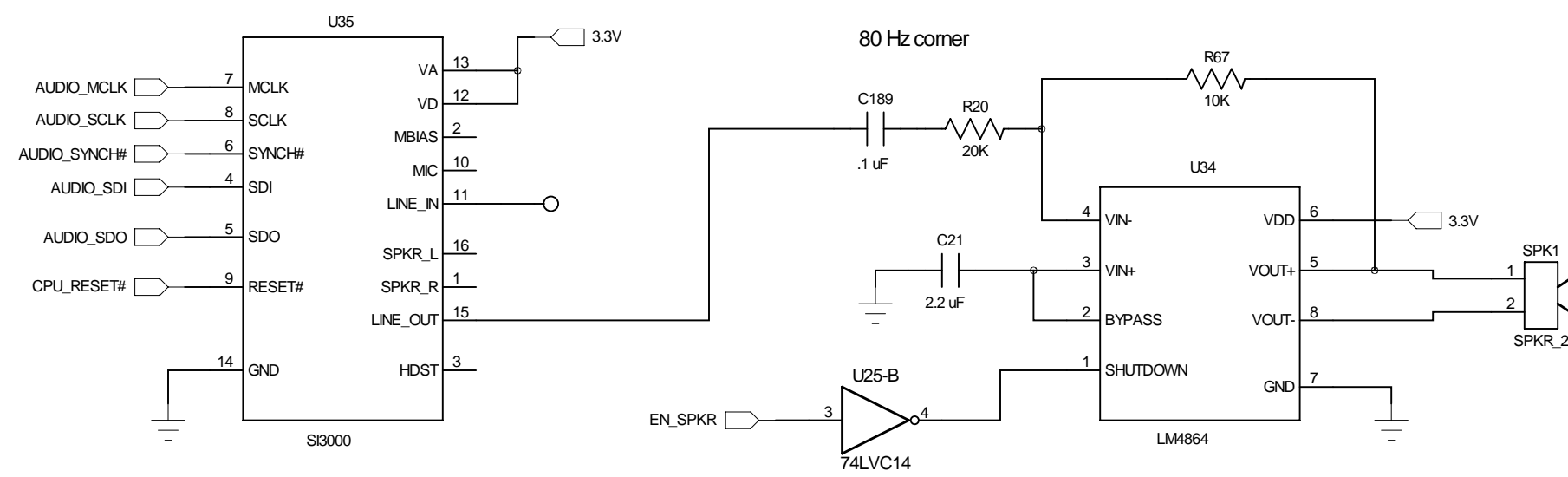
Right LED (Amber)
100 Mbit
Left LED (Green)
Link / Activity

Technologic Systems	Date	Oct. 7, 2008
Title: TS-7390 5V Power Supply		
Rev.	Designer	Sheet 7 of 8

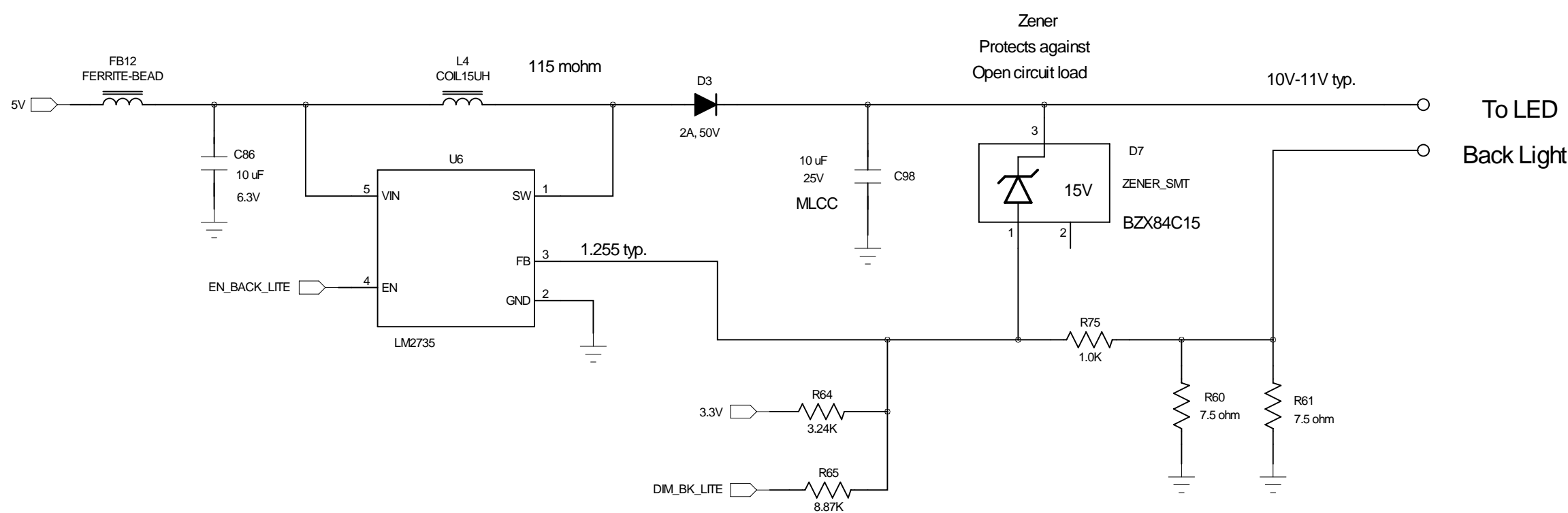
Touch Screen Controller



SPKR DAC



BackLight Power



87% typ. eff. at 200 mA load
(12V out) per data sheet

744 mV is high setting (198 mA)
333 mV is low setting (88 mA)

200 mA is maximum continuous
that LED BackLight is rated at.