TS-NVRAM2 Manual

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All modifications from previous versions are listed in the appendix.

Limited Warranty

Technologic Systems warrants this product to be free of defects in material and workmanship for a period of one year from date of purchase. During this warranty period Technologic Systems will repair or replace the defective unit in accordance with the following instructions:

- Contact Technologic Systems and obtain a Return Material Authorization (RMA) number and a copy of the RMA form.
- Fill out the RMA form completely and include it and dated proof of purchase with the defective unit being returned. Clearly print the RMA number on the outside of the package.

This limited warranty does not cover damages resulting from lightning or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Technologic Systems be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

Repairs made after the expiration of the warranty period are subject to a flat rate repair charge and the cost of return shipping. Please contact Technologic Systems to arrange for any repair service.

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1. Introduction

The TS-NVRAM2 is a PC/104 expansion card that adds up to 2 MB of nonvolatile high-speed battery-backed RAM. It can be arranged as 8 bit or 16 bit wide memory and can be configured as paged memory or linear memory. The TS-NVRAM2 eliminates any wear-out failure and write cycle latency inherent in all Flash devices

This product uses a multi-layer PCB with power and ground planes to minimize noise and EMI issues. The TS-NVRAM2 only requires a single 5V power supply.

2. Getting Started

X86 Architecture

Install only jumpers 3 and 4 on the TS-NVRAM2, this will put the board in 8-bit mode and set the base address for all registers in the I/O space at 0x140. After a system reset, only the eight I/O registers will appear on the PC/104 bus (no memory range will be decoded) -- this will avoid any conflicts with any other devices. Next write out 0x46 to I/O location 0x145 (Mode Register). This will configure the TS-NVRAM2 to use paged memory and will make it appear in memory space at 0xD0000 to 0xD7FFF (a 32 KB window). This memory range is suggested, since this range is typically free in most x86 platforms, but any 32KB range from 0xA0000 thru 0xDFFFF can be selected (see Mode register details). Now the NVRAM memory can be accessed at the memory addresses 0xD0000 to 0xD7FFF. Any one of the 64 pages can be selected by writing to the page register at I/O location 0x144. Since each page is 32 KB and there are 64 pages this allows access to all 2MB of NVRAM. Up to four TS-NVRAM boards can be installed to get up to 8MB of non-volatile memory.

TS-ARM Architecture

Ensure no jumpers are installed on the TS-NVRAM2 board. This will put the board in 16-bit mode and will set the base address for all registers accesses in the I/O space to 0x11E0_0140. After system reset, only the eight I/O registers will appear on the PC/104 bus (no memory range will be decoded) -- this will avoid any conflicts with any other devices. Next write out 0x80 to 0x11E0_0145 (Mode Register). This will configure the TS_NVRAM2 to use linear memory and will make it appear in the memory space at 0x2A80_0000 to 0x2A9F_FFFF (a 2MB range). Two TS-NVRAM2 boards could be used in a system to get 4MB of linear non-volatile memory.

3. PC/104 Bus Interface

The TS-NVRAM2 features a single 64-pin PC/104 connector that allows standard 8-bit data bus access. This is used to support the standard 8-bit mode for any PC/104 system. It is possible to access the TS-NVRAM2 board in full 16-bit mode if using a TS-72xx product. These Technologic System ARM-based SBC products can do full 16-bit data accesses using only the 64-pin connector.

A Xilinx Programmable Logic Device (PLD) is used for all address decode and other logic required to interface the PC/104 bus to the Maxim DS1321controller as well as the 2 Megabytes of RAM. This allows for a great amount of flexibility for adding any special options that may be required in the future.

4. Maxim DS1321 Controller

The TS-NVRAM2 uses a Maxim DS1321 controller, which performs the function of controlling whether the PC/104 5V power is used to power the SRAM chips, or whether a 3V lithium battery is used. When input power falls below 4.25 volts, the DS1321 will switch the SRAM chips over to using the lithium battery so that the memory chips always see uninterrupted power. While input power is below 4.25 volts, all accesses to the SRAM chips are inhibited. This prevents any data corruption during power failures.

In addition to battery-backup support, the DS1321 performs the important function of monitoring the remaining capacity of the lithium battery and providing a warning before the battery reaches end-of-life. Because the open-circuit voltage of a lithium backup battery remains relatively constant over the majority of its life, accurate battery monitoring requires loaded-battery voltage measurement. The DS1321 performs such measurement by periodically comparing the voltage of the battery to an internal precision reference with the battery loaded. The battery is loaded by switching on an internal resistive load for a very short time interval during which the measurement is made. If the battery voltage falls below the reference voltage under such conditions, the battery will soon reach end-of-life. When the DS1321 sets its battery-warning pin, the PLD will turn on the red LED. (Note: the red LED is powered by the main 5V power and has no effect on battery life). The LED register will also indicate that the battery needs replacing.

In most applications, the battery will never need replacing since the standby current for a 2MB SRAM bank is typically in the 2-4 microampere range. Using the 600 mA-hour lithium battery (CR2450 coin cell), this results in a typical 15-30 year life span. But if the unit is operated at high temperatures for its entire life, this will lower the battery life. For example, if the TS-NVRAM2 board is operated at 70 degrees Celsius continuously, the lithium battery is likely to fail after 3-4 years.

5. Registers

ID #1

7	6	5	4	3	2	1	0
ID_1							

Address: Base + 0 (Read Only)

Definition: This register allows one to determine the board ID.

Bit Description: *ID_1*: Identification byte is hard coded to 0x77.

ID #2

7	6	5	4	3	2	1	0
ID_2							

Address: Base + 1 (Read Only)

Definition: This register allows one to determine the board ID.

Bit Description: *ID_2*: Identification byte is hard coded to 0xD9.

PLD Version

7	6	5	4	3	2	1	0
REV							

Address: Base + 2 (Read Only)

Definition: This register allows one to determine the revision of the PLD.

Bit Description:

REV: The revision number of the PLD.
0x01 = Initial Revision

LED Status

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GREEN	RED

Address: Base + 3 (Read Only)

Definition: This register allows one to determine the state of the LEDs.

Bit Description:

GREEN: When this bit is set it indicates the green led is on, when this bit is clear it indicates the green LED is off. The green LED is on when the PC/104 power is greater than 4.5V.

RED: When this bit is set it indicates the red led is on, when this bit is clear it indicates the red LED is off. If the red LED is on, the battery is near failure.

RSVD: Reserved.

Page Register

7	6	5	4	3	2	1	0
RSVD	RSVD	PAGE_SELECT					

Address: Base + 4 (Read/Write)

Definition: This register allows one to select the current page when in paged mode. At reset PAGE_SELECT is set to 0x00.

Bit Description:

PAGE_SELECT: When in paged mode this register allows one to select one of 64 pages for NVRAM access (each page is 32 KB). This allows up to 2 MB of NVRAM.

RSVD: Reserved.

Mode Register

7	6	5	4	3	2	1	0
LINEAR	PAGED	TEST_MODE	RSVD	DECODE	MEM_SELECT		

Address: Base + 5 (Read/Write)

Definition: This register provides various system configuration options. This register defaults to zero indicating NVRAM doesn't appear anywhere in memory space after power up or a system reset.

***Note*:** When the LINEAR bit is set PAGED and MEM_SELECT bits 1 through 3 are ignored.

Bit Description:

LINEAR: When this bit is set NVRAM appears as linear memory. This mode is not compatible with x86-based systems.

PAGED: When this bit is set NVRAM appears in a 32 KB window. One can use the PAGE_SELECT register to select the current page. This bit must be set on x86-based systems.

TEST_MODE: This bit is used for factory testing to change between 8 and 16 bit mode.

DECODE: When this bit is clear only address lines 15 through 19 are used for decoding (recommended for x86 platforms). When this bit is set address lines 15 though 21 are used for decoding (recommended for TS-ARM based platforms).

MEM_SELECT: When in paged mode this register can be used to select the base address. If the DECODE bit is set, base addresses are as follows.

Note: TS-ARM platforms only

MEM_SELECT	Base address
000	0x1180_0000
001	0x1181_0000
010	0x1182_0000
011	0x1183_0000
100	0x11B0_0000
101	0x11B1_0000
110	0x11B2_0000
111	0x11B3_0000

If the DECODE bit is clear, base addresses are as follows.

Note: 8-bit mode only

MEM_SELECT	Base address
000	0xA0000
001	0xA8000
010	0xB0000
011	0xB8000
100	0xC0000
101	0xC8000
110	0xD0000
111	0xD8000

When in linear mode MEM_SELECT bit 0 determines the base address.

Bit 0, MEM_SELECT	Memory Width	Base Address
0	16	0x2A80_0000
1	16	0x2AA0_0000

RSVD: Reserved.

Jumpers

7	6	5	4	3	2	1	0
RSVD	RSVD	JP5	JP4	RSVD	JP2	JP1	RSVD

Address: Base + 6 (Read Only)

Definition: This register allows one to determine the state of the jumpers.

Bit Description:

JP5: This bit indicates the state of JP5, set indicates the jumper is on.

JP4: This bit indicates the state of JP4; set indicates the jumper is on.

JP2: This bit indicates the state of JP2; set indicates the jumper is on.

JP1: This bit indicates the state of JP1; set indicates the jumper is on.

RSVD: Reserved.

6. Jumpers

JP1 and JP2 determine the base address, base address configurations are shown below.

Base Address	0x140	0x148	0x160	0x168
JP1	Off	On	Off	On
JP2	Off	Off	On	On

JP3 and JP4 determine data width, data width configurations are shown below (JP3 and JP4 must both be on or must both be off).

Data Width	8-Bit	16-Bit	Invalid	Invalid
JP3	On	Off	Off	On
JP4	On	Off	On	Off

7. Current Drain

The TS-NVRAM2 uses approximately 50 mA of current from the PC/104 bus 5V supply. When the PC/104 5V is not present, the RAM chips are powered by the lithium battery (CR2450). Approximately 2-4 uA of backup current is required to power the RAM chips in this mode. This can be measured with a DVM by measuring the voltage at the test point labeled “Drain Test” with respect to ground. Every microamp of drain current from the battery causes a negative 100 microvolts of voltage.

8. Temperature Range

The TS-NVRAM2 is available in both standard temperature (-20 to +70 degrees Celsius) and in extended temperature range of –40 to +85 degrees Celsius.

Appendix A Manual Revisions

Date	Revision Number	Revision
September 09, 2005	0.9	Preliminary release
September 16, 2005	1.0	Initial release
June 05, 2009	1.1	Updated address