

10/100 Ethernet

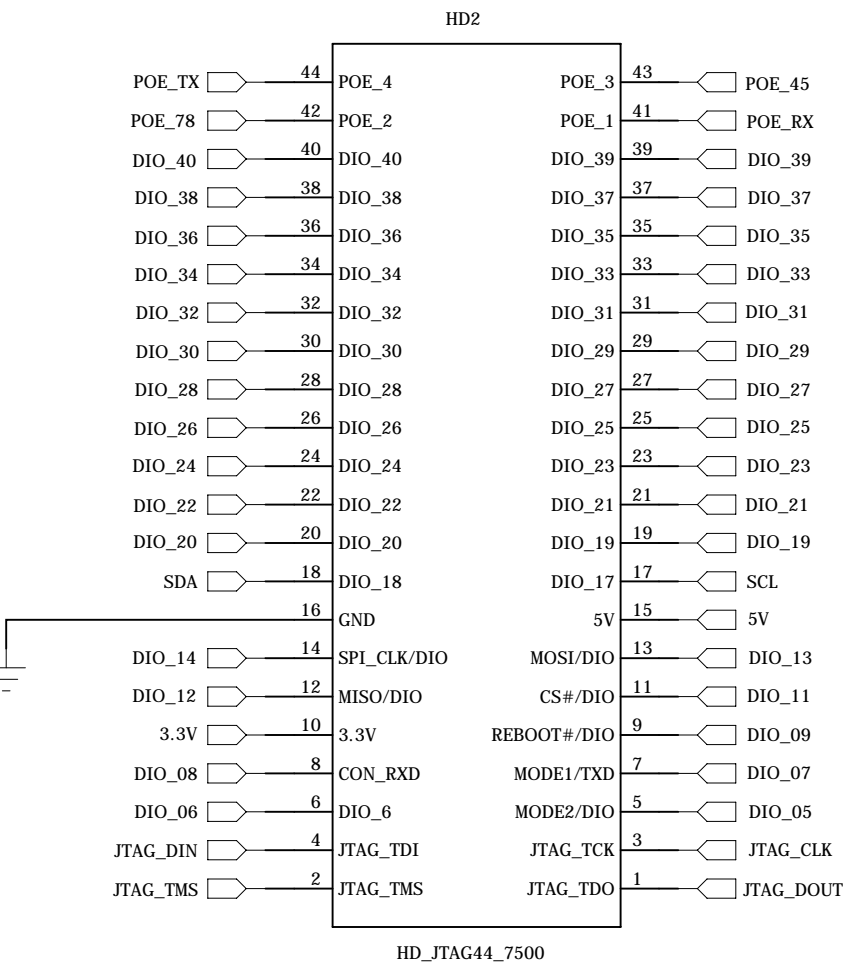
Reset Latch

POR

Left LED (Green)
Link / Activity

Technologic Systems	Date	May 30, 2009
Title: TS-7500 CPU, Ethernet, POR		
Rev:	Designer	RLM
Sheet		1 of 4

44-Pin DIO Header (Bottom)



Mode 1	Mode 2	TS-7500 Boots from
1	1	SPI Flash
0	1	SD card
1	0	Off-board Flash
0	0	Reserved

0 0 also boots from off-board Flash, but may be changed in the future

SPI bus default to DIO But can be switched to SPI function

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Console always is enabled after power up (or reset) but can be switched to DIO after done booting

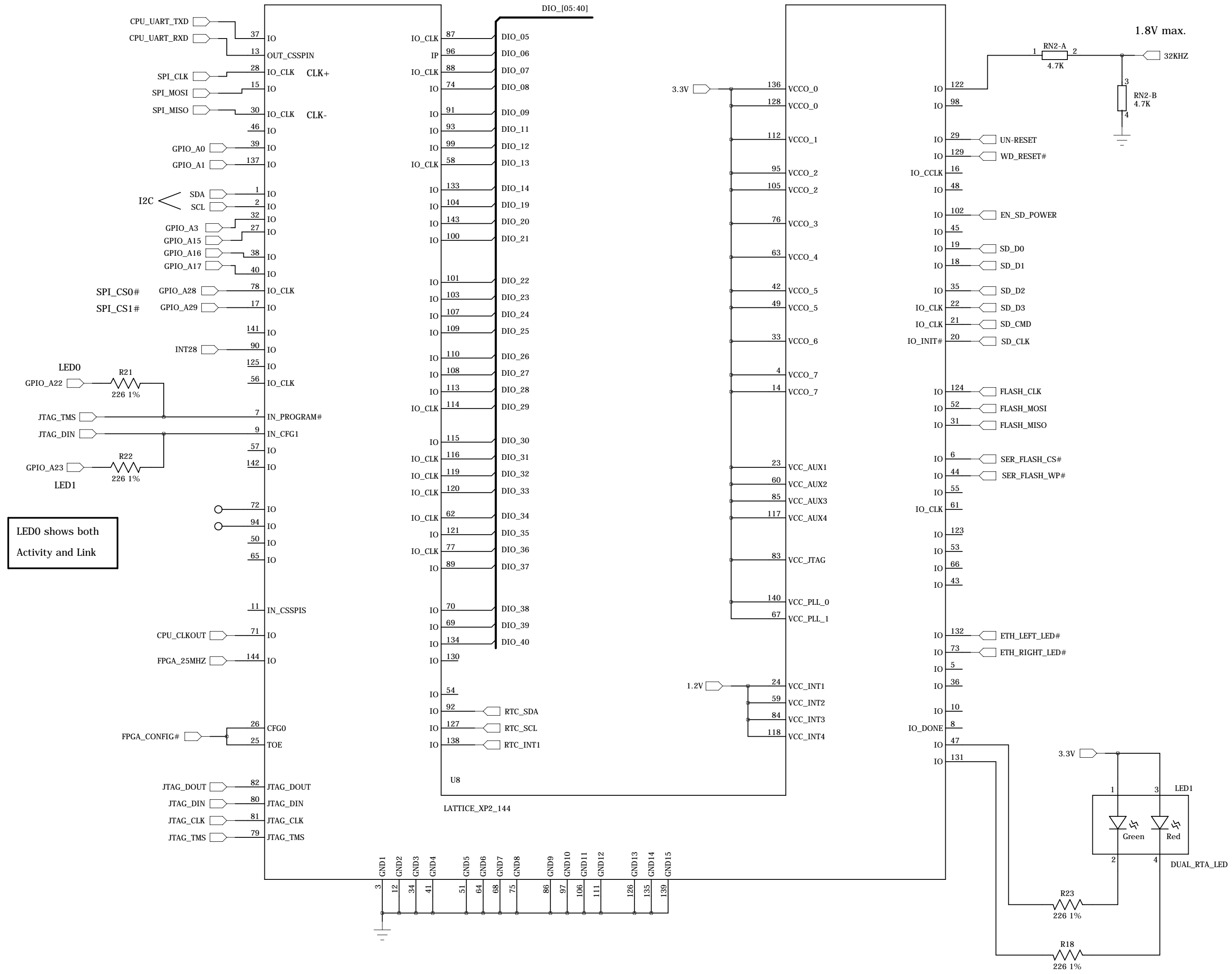
Reboot# pin (DIO_09) defaults to DIO But can be switched to Reset function

LEDO shows both Activity and Link

Pull-up and pull-down resistors are 6 to 30K ohms

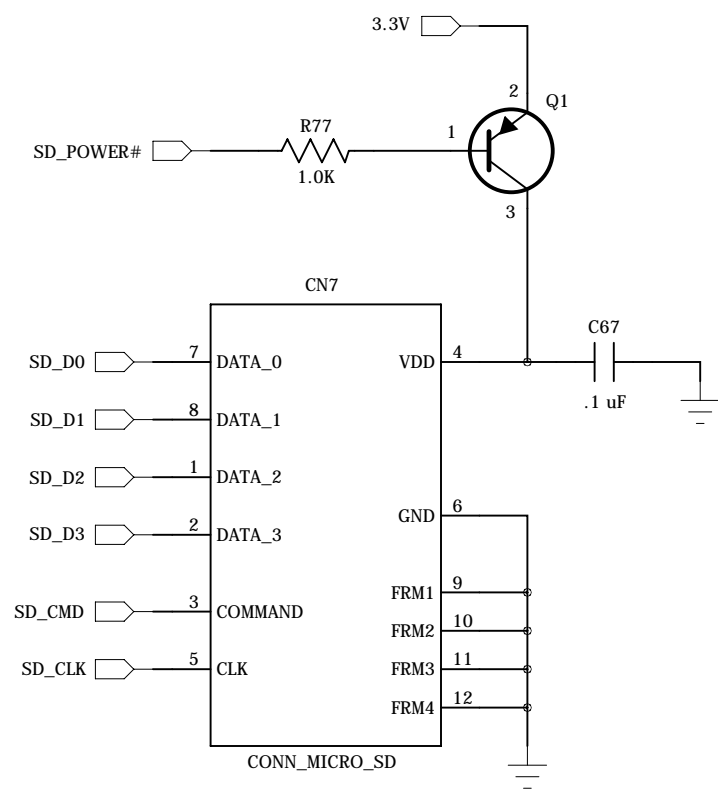
FPGA with 5000 LUTs

XP2-5 has:
5K LUTs 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 ms
input PLL clock = 10 MHz min

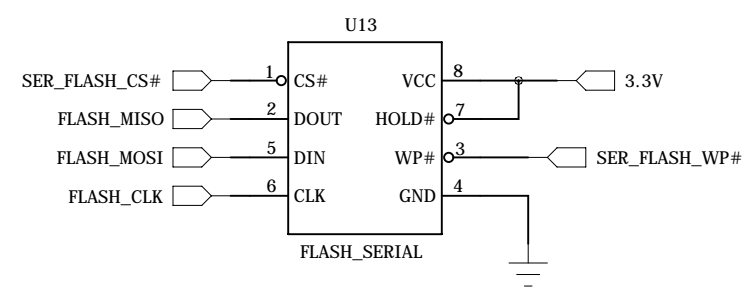


Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

Micro SD Card Socket



4MB Serial Flash



DDR RAM Notes

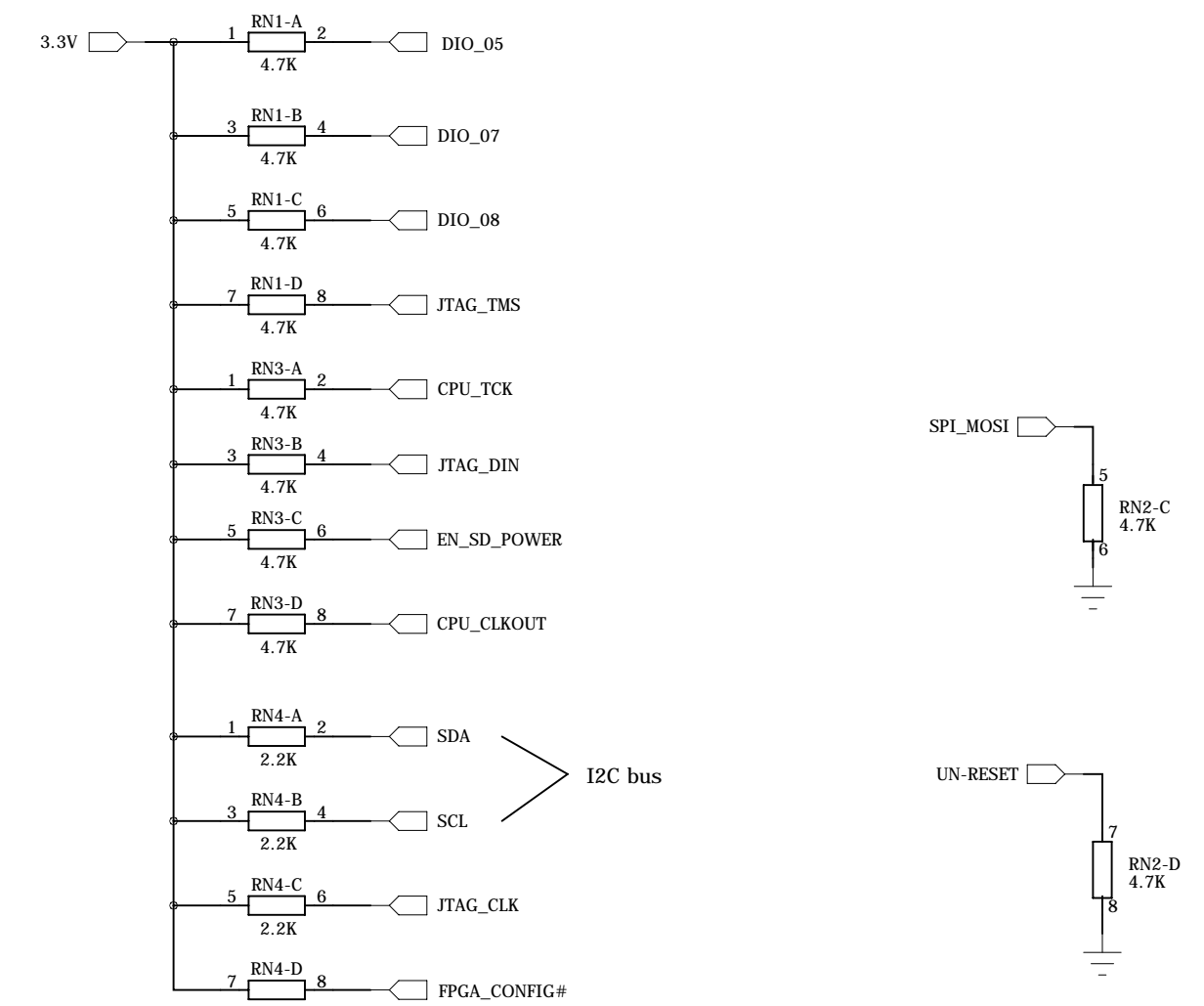
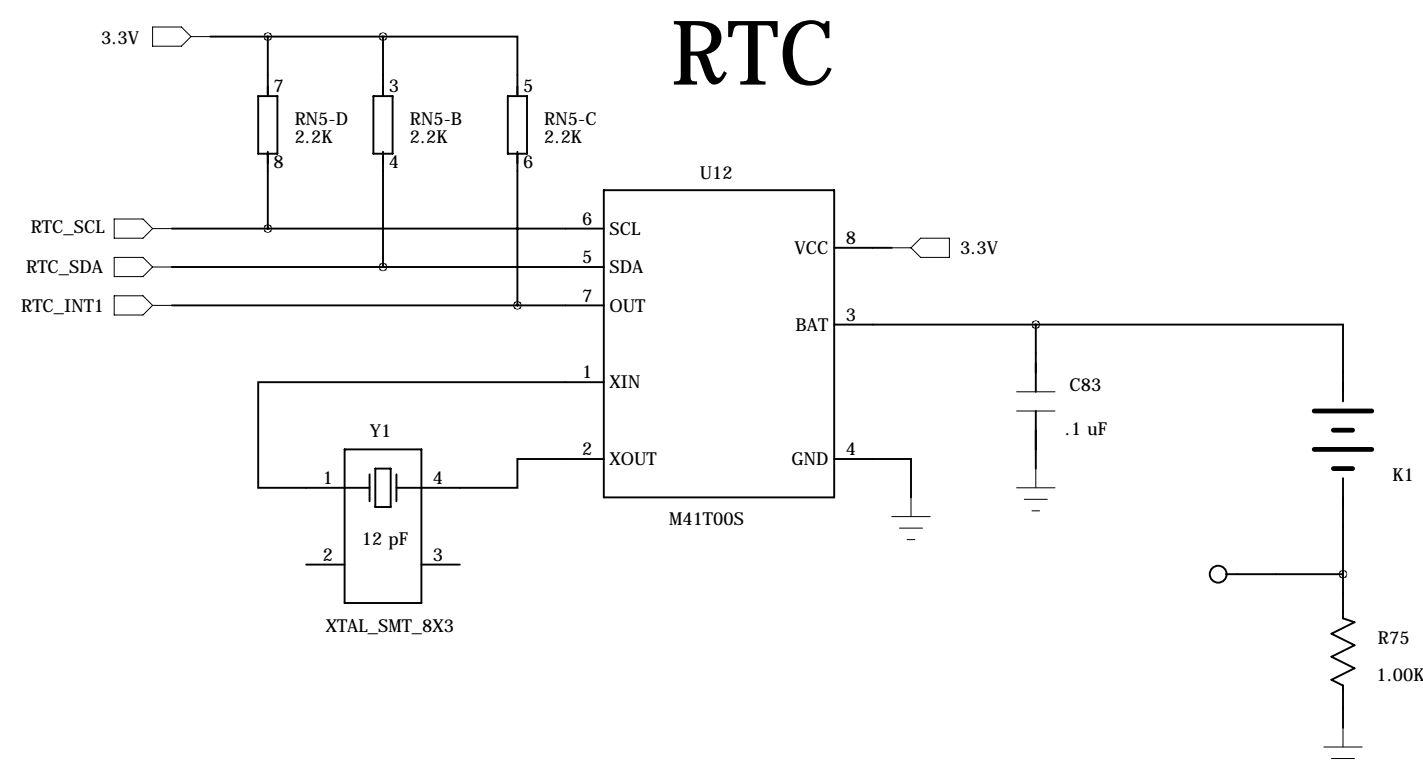
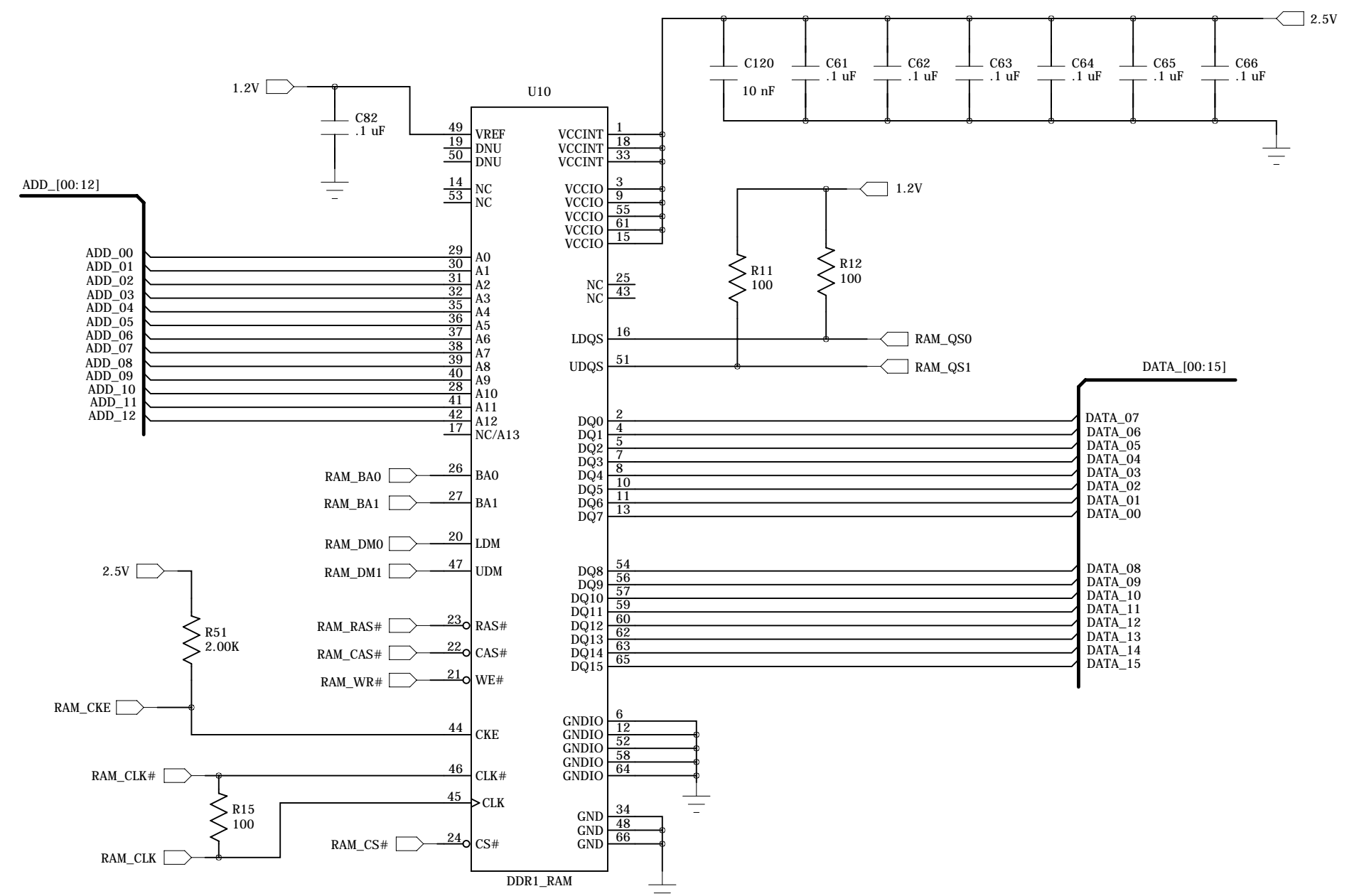
The DDR clock differential pair is the most critical trace on the entire board

The data lines in each byte lane can be swapped on the RAM chip for optimal layout
Example: D0 and D5 can be swapped, but not D7 and D8

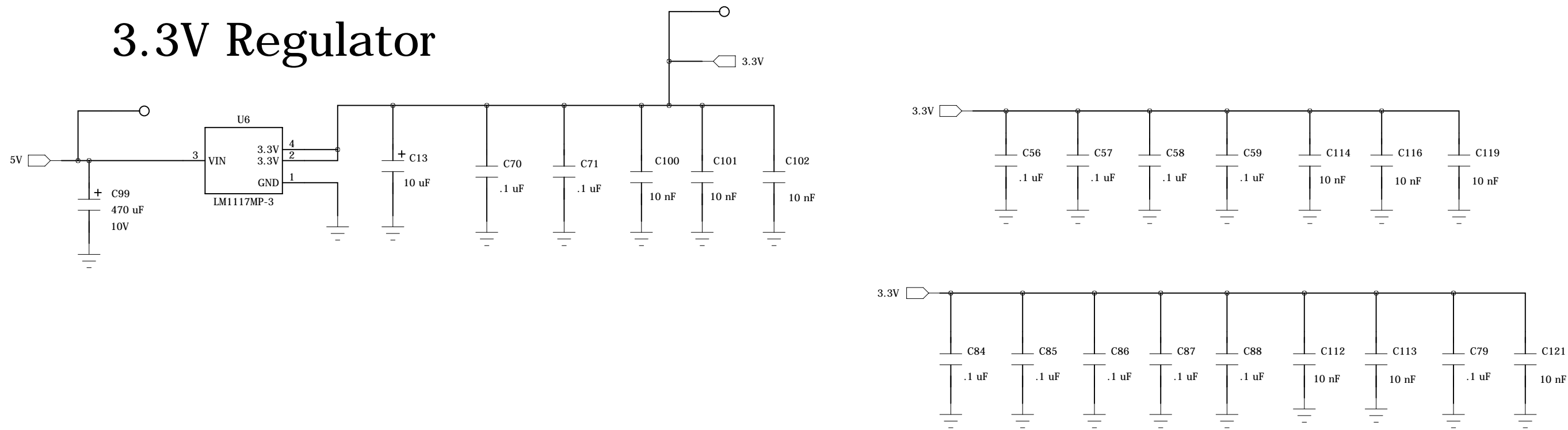
The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm

Address and Command signals can be grouped together, but must be isolated
from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer

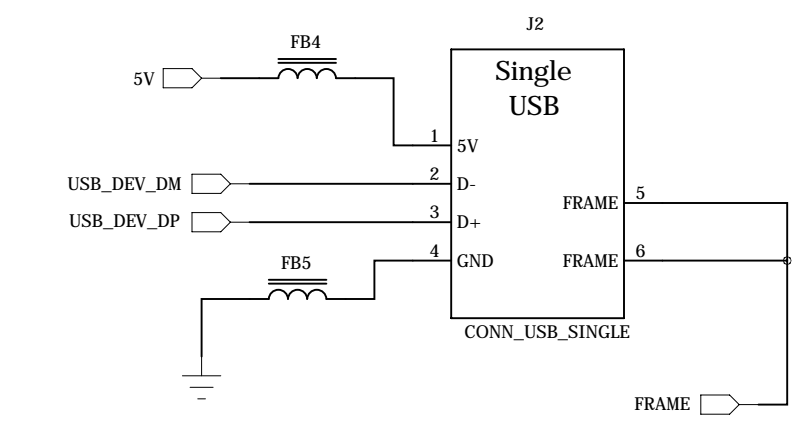
64 Mbyte DDR1 SDRAM



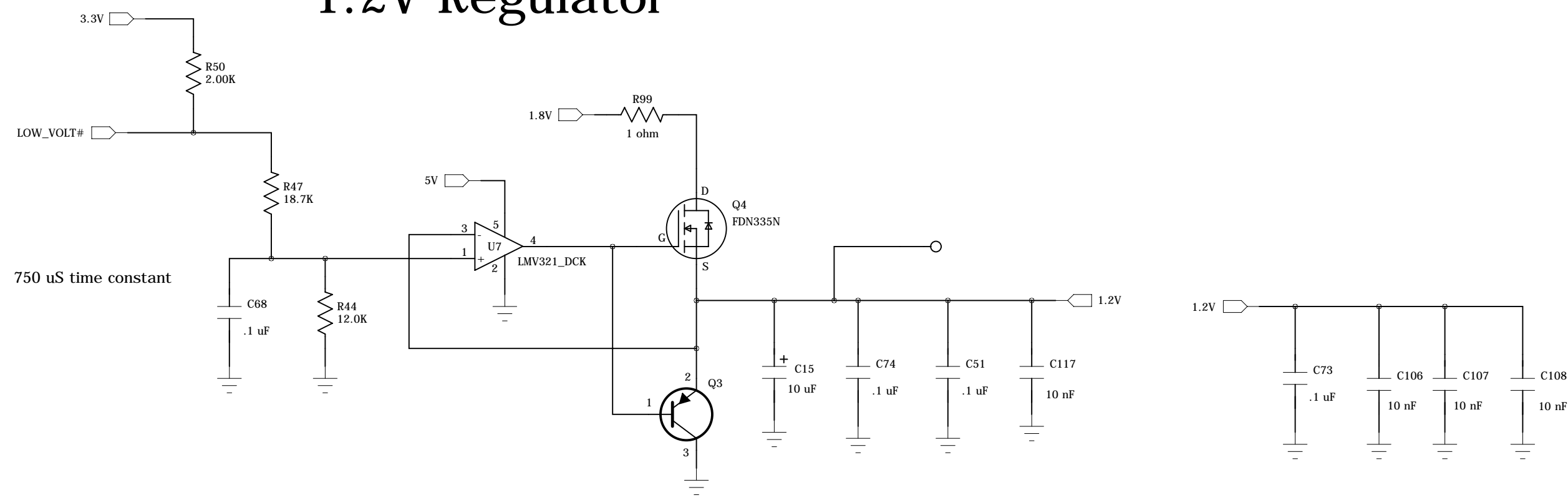
3.3V Regulator



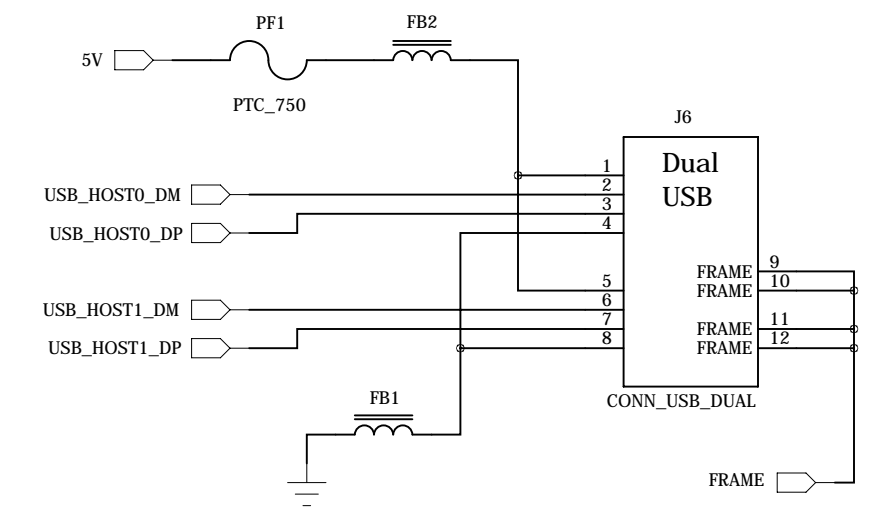
USB Device Port



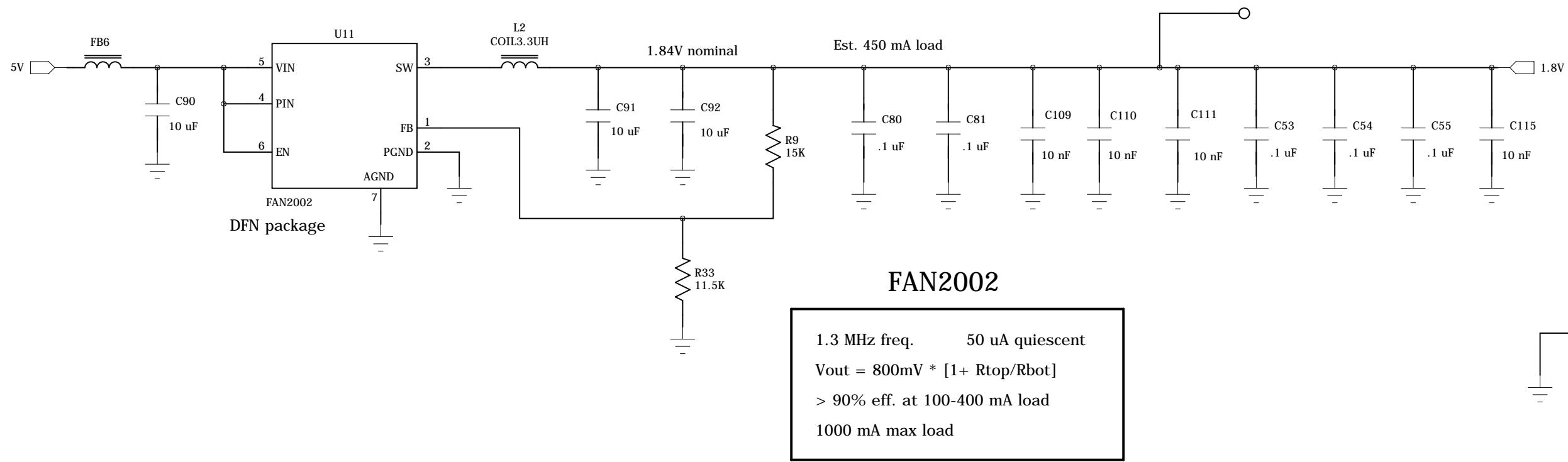
1.2V Regulator



USB Host Ports



1.8V Regulator



2.5V Regulator

