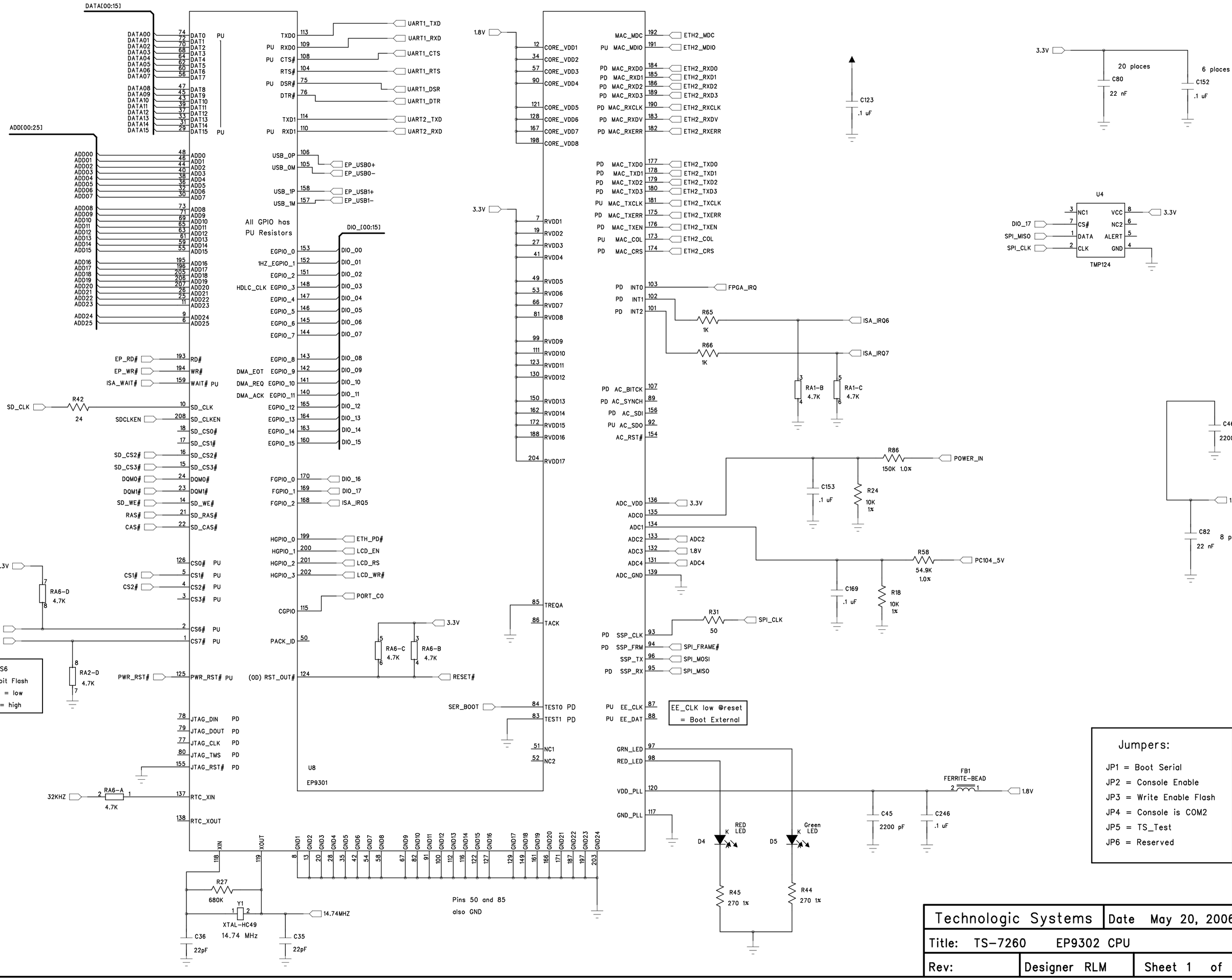
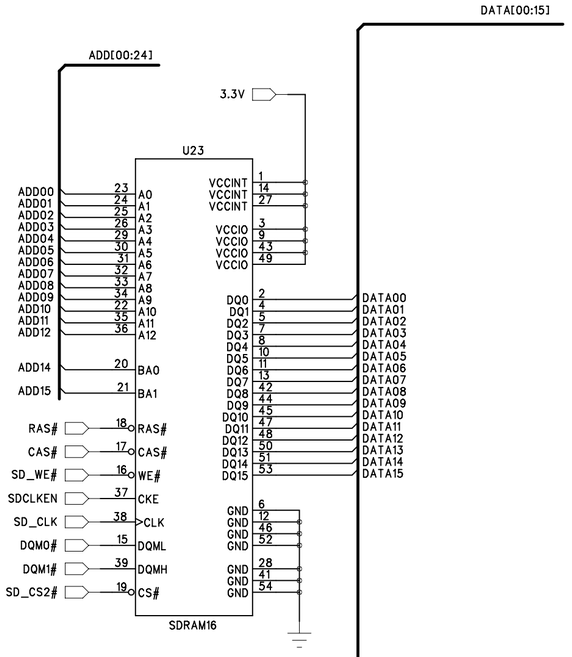
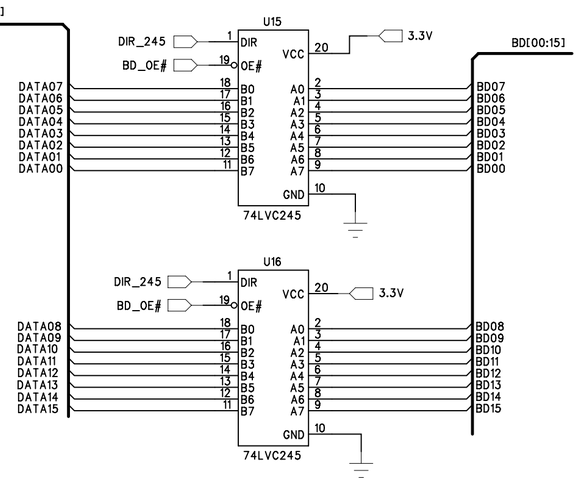
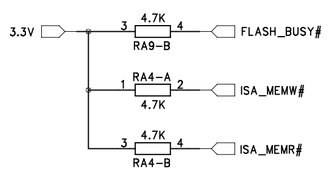

DATA[00:15]
ADD[00:25]
All GPIO has
PU Resistors
DIO_[00:15]
U8
EP9301
U4
TMP124
20 places
6 places
8 places
CS7 and CS6
Select 16-bit Flash
when CS7# = low
and CS6# = high
EE_CLK low @reset
= Boot External
Pins 50 and 85
also GND
Jumpers:
JP1 = Boot Serial
JP2 = Console Enable
JP3 = Write Enable Flash
JP4 = Console is COM2
JP5 = TS_Test
JP6 = Reserved
Technologic Systems
Date May 20, 2006
Title: TS-7260 EP9302 CPU
Rev:
Designer RLM
Sheet 1 of 6

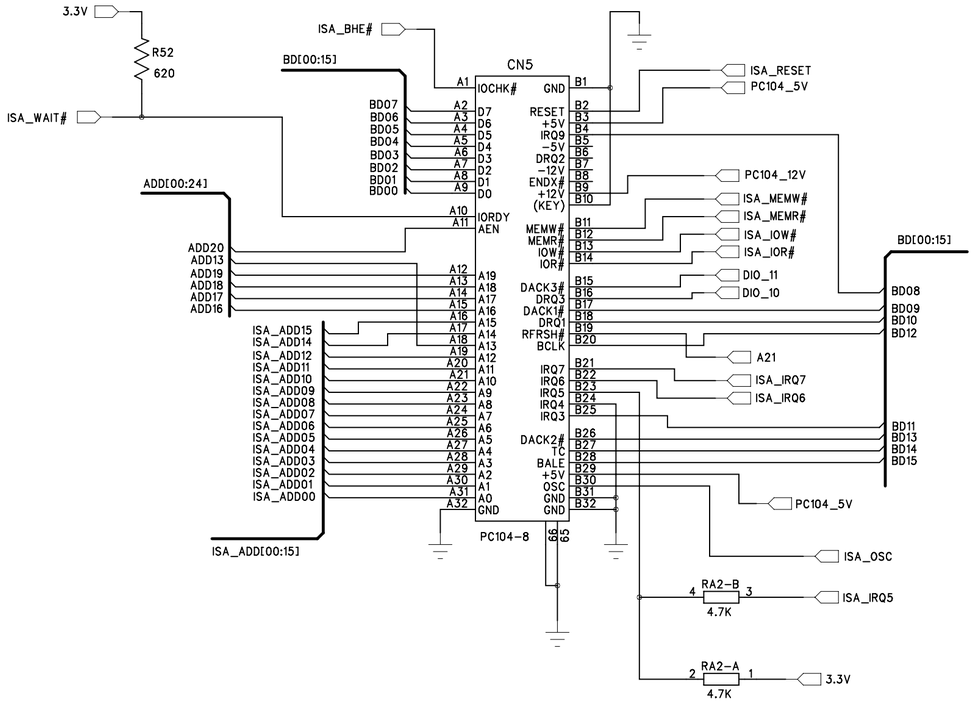
SDRAM





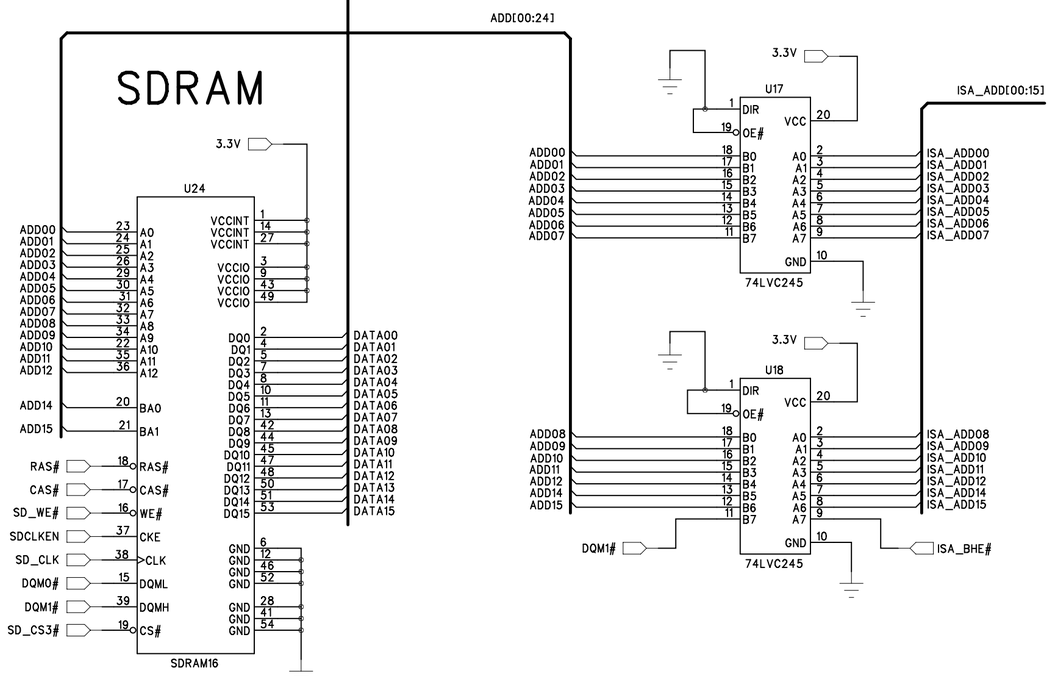


PC/104 Connector

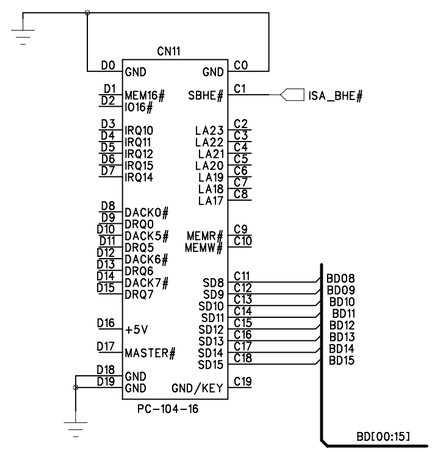


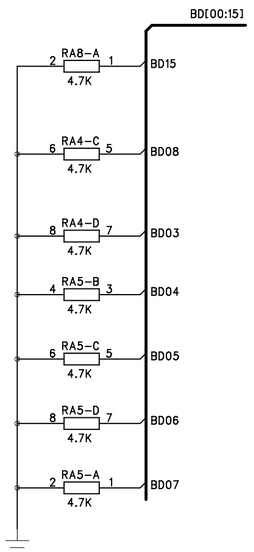
IRQ6 and IRQ7 have Resistor pull downs

SDRAM



PC/104 40-pin Connector



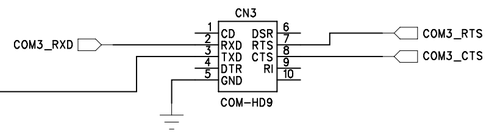


Data Bus Pull-Down Resistors

Technologic Systems		Date May 20, 2006
Title: TS-7260 RAM, Flash, PC/104		
Rev:	Designer RLM	Sheet 2 of 6

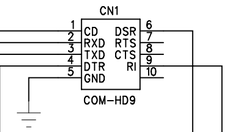
3.3V RS-232
SP3239EEA
$1.19 46/tube

COM3 Header



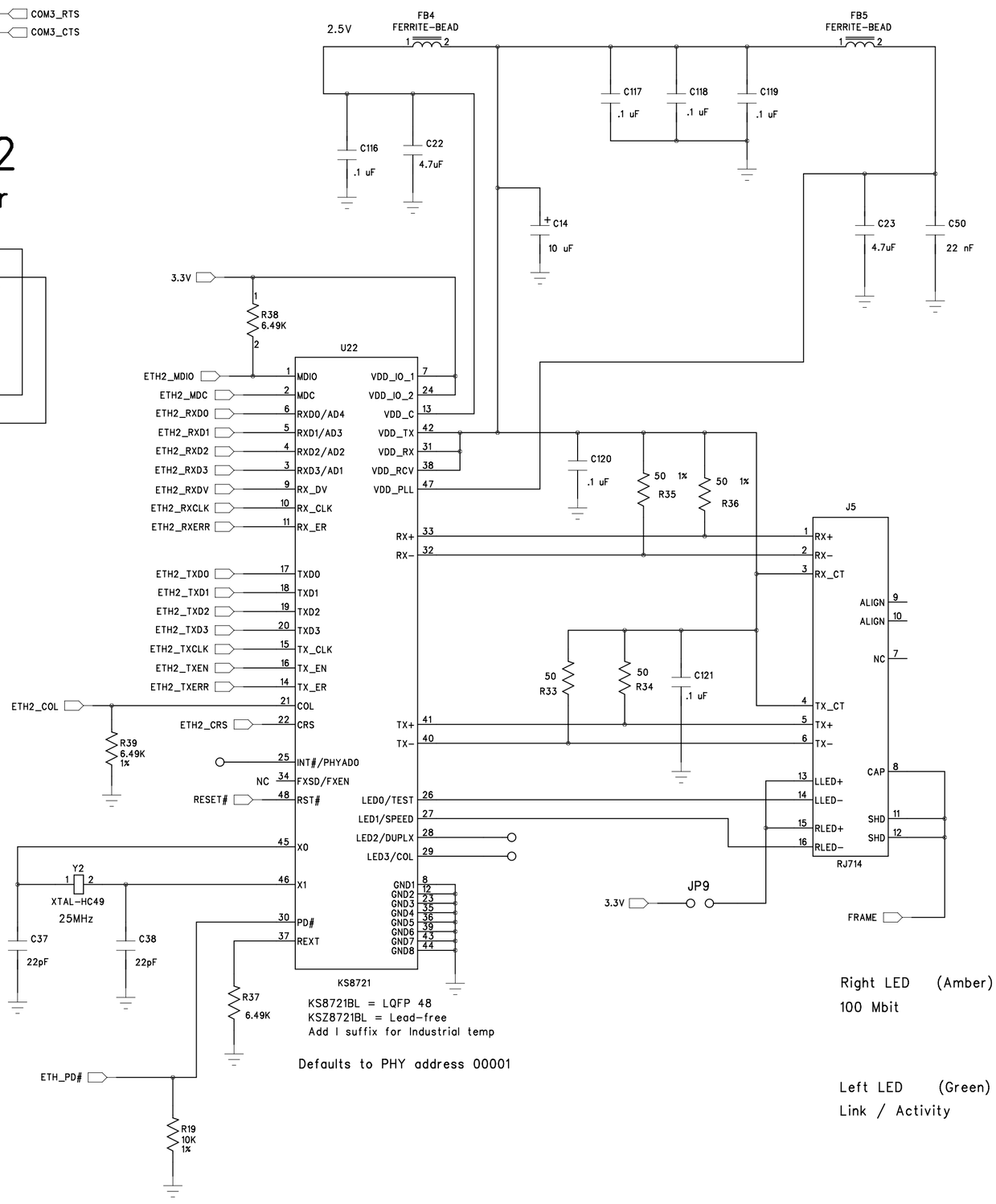
COM1

COM2 Header



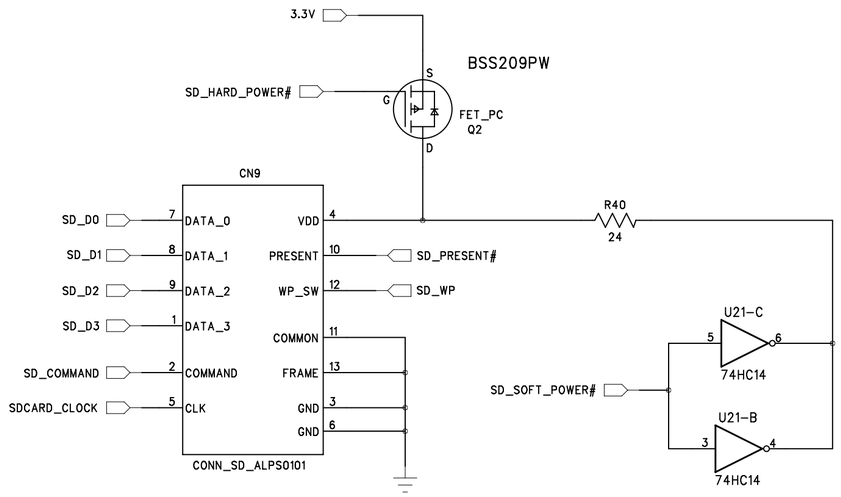
3.3V RS-485
SP3072EEN-L (Leadfree)
$1.05 98/tube

10/100 Ethernet

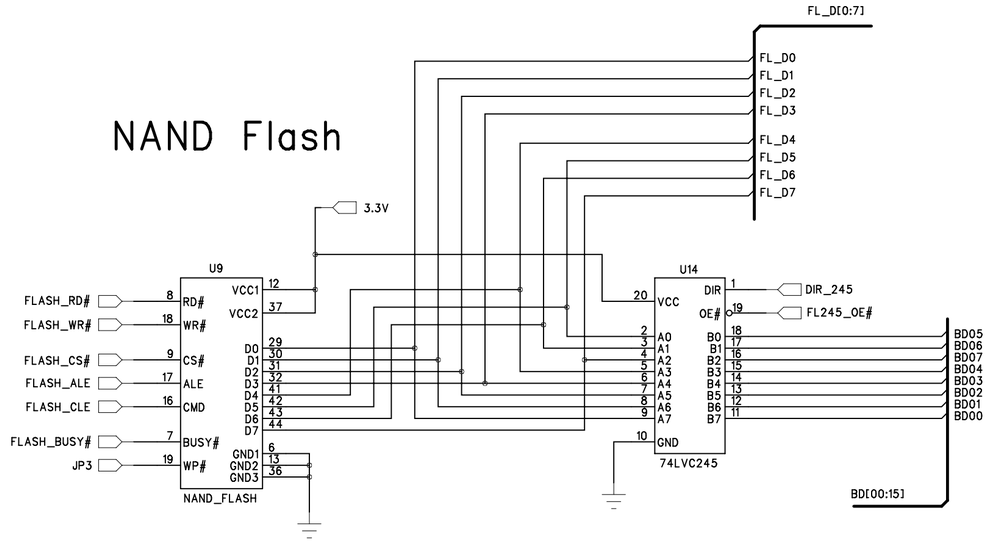


Technologic Systems	Date May 20, 2006	
Title: TS-7260 Ethernet, COM ports, USB		
Rev:	Designer RLM	Sheet 3 of 6

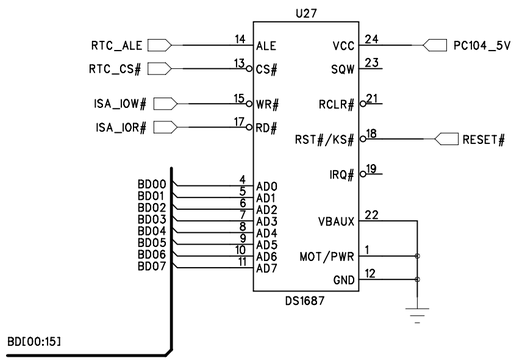
SD Card Socket



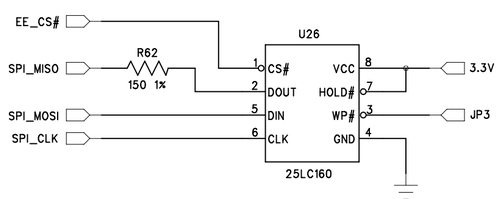
NAND Flash



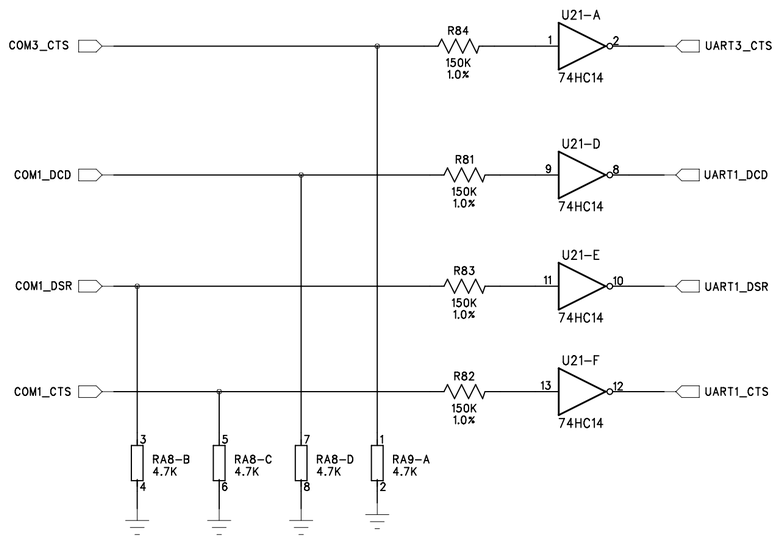
Real Time Clock



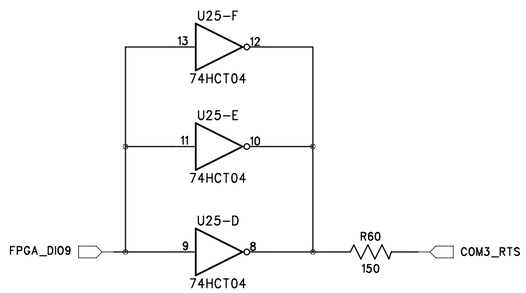
Boot EEPROM



3.3V Powered



5V Powered



Technologic Systems		Date May 20, 2006
Title: TS-7260 NAND Flash, EEPROM, RTC		
Rev: 1.0	Designer RLM	Sheet 4 of 6

4.5–20V Power In

BLM21PG221SN1D
FB2
FERRITE–BEAD
220 ohm @100MHz
50 milliohm DC
POWER_IN
CN4
VCC
GND
POWER2PIN
JP7
JP8
PC104_12V
10 uF
25V
MLCC
C94
PC104_5V
R23
10K
1%
Q1
3.3V
MMBT3906
D1
BAT54–S
JP7_ON
R57
54.9K
1.0%
PWR_RST#

5V Load

U25–C
U25–A
U25–B
74HCT04
ISA_RST
R46
270 1%
PC104_5V

5V Boost Supply

3.3V
C31
4.7uF
L3
COIL12UH_SMT
12_15 uH
D8
PC104_5V
U19
VIN
SW
EN
SOFT
FB
FREQ
COMP
GND
MP1542
EN_PC104_5V
R51
620
D2
BAT54–S
LOW_VOLT#
C48
22 nF
Vref = 1250 mV
R15
30.1K
1%
C47
2200 pF
R21
10K
1%
R20
10K
1%
C96
10 uF
25V
MLCC
C97
10 uF
25V
C99
330 uF
25V
optional
Vout = Vref * [(R15 / 10K) + 1]

3.3V Power Supply

10uF 25V MLCC
TDK C3225X7R1E106K = 10%
TDK C3225X7R1E106M = 20%
0.16 @ 1K Reel Future

FB6
FERRITE–BEAD
C170
.1 uF
PC104_5V
D3
BAT54–S
C49
22 nF
L1
COIL12UH_SMT
12_15 uH
D9
U3
BOOST
VIN
SW
EN
FB
SOFT
COMP
GND
MP2309
Ref = 923 mV
R13
26.1K
1%
Vout = [1 + (R13 / 10K)] * Vref
R22
10K
1%
C16
3.3 nF
R12
7.50K
1%
C93
22 nF
10 uF
25V
MLCC
C95
R56
54.9K
1.0%
R55
54.9K
1.0%
C157
.1 uF
R70
1.0K
SHUTDOWN#
C25
4.7uF
C26
4.7uF
C27
4.7uF

4.7 uF is 6.3V 20%
TDK C1608X5R0J475M
5.5 cents @TTI

1.8V Power Supply

Vout = 0.5V [1 + R1 / R2]
U6
VIN
SW
EN
FB
GND
LM3670
LM3670MF–ADJ
L2
COIL12UH_SMT
12_15 uH
FB8
FERRITE–BEAD
1.8V
Ref = 500 mV
C12
100 pF
R85
150K
1.0%
R54
54.9K
1.0%
2.74 RATIO = 1.87V
C19
4.7uF
C20
4.7uF
C21
4.7uF
C29
4.7uF
C30
4.7uF
C32
4.7uF
FB7
FERRITE–BEAD
220 ohm @100MHz
3.3V
C28
4.7uF
C24
4.7uF

DIO Port

3.3V
DIO_[00:15]
CN8
HEADER16
SPI_CLK
SPI_MOSI
SPI_MISO
DIO_16
SPI_FRAME
PORT_C0
DIO_15
DIO_14
DIO_13
DIO_12
DIO_11
DIO_10
DIO_09
DIO_08
X2
X1
MT125

LCD Port

DIO_[00:15]
HD14PIN
CN7
DIO_06
DIO_04
DIO_02
DIO_00
DIO_07
DIO_05
DIO_03
DIO_01
R73
1K
R74
1K
R72
1K
R75
1K
R71
1K
R76
1K
R69
1K
R68
1K
LCD_WR#
R32
51.1 1%
LCD_EN
LCD_RS
R50
620
4.7K
RA2–C

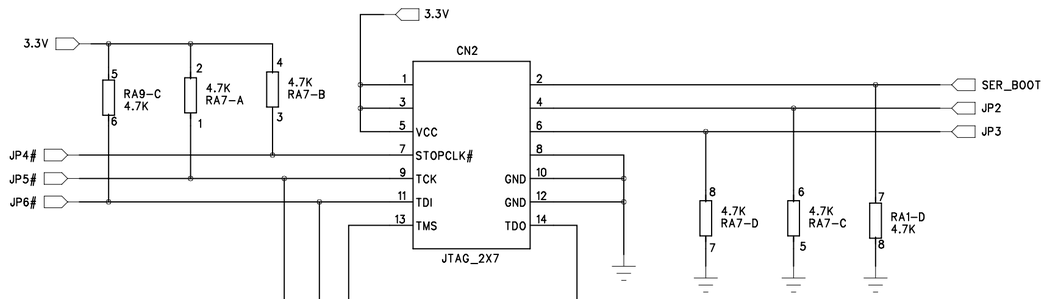
PC104_5V
U13
EN_A
FLT_A#
OUT_A
EN_B
FLT_B#
OUT_B
5V
GND
MIC2026–1BM
EN_LCD_5V
EN_USB_5V
USB_5V
LCD 5V Power

140 mohm on resistance
1mS soft start from Enable
About 1.2 Amp current limiting

Sipex 2526A–1EN–L
is 2nd source

Technologic Systems	Date May 20, 2006	
Title: TS–7260 Power, DIO, LCD ports		
Rev:	Designer RLM	Sheet 5 of 6

JTAG



Jumpers:

JP1 = Boot Serial
JP2 = Console Enable
JP3 = Write Enable Flash
JP4 = COM2 is Console
JP5 = TS_Test
JP6 = Reserved

MAX2 current drain

Icore during power up = 40 mA typical
Icore idle = 2 mA (no clocks)
Icore with 14.7 MHz clocking is 4-6 mA

Current for 3.3V is dynamic only
(probably 2-5 mA only)

MAX2_570 requires 300 uS to copy Flash into RAM after Vcore > 1.5V

XDIO_DIO9 also drives COM3_RTS
XDIO_DIO9 is always an output

The XDIO pins can optionally support these signals

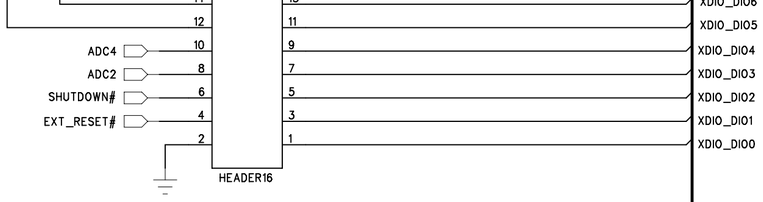
Pin 1 = COM3 TXD
Pin 3 = COM3 RXD
Pin 5 = Aux1 TXD
Pin 7 = Aux1 RXD
Pin 9 = Aux2 TXD
Pin 11 = Aux2 RXD
Pin 13 = Aux1 TX shifting
Pin 15 = Aux2 TX shifting

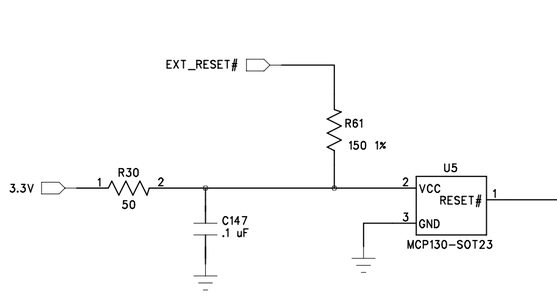
The XDIO pins can optionally support an SD card socket

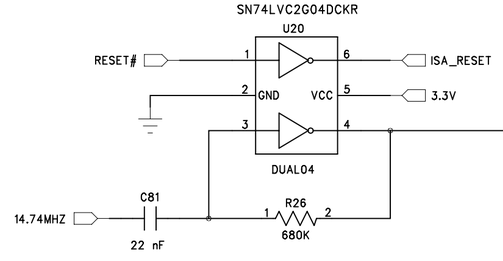
Pin 1 = XDIO_0 SD Data_1
Pin 3 = XDIO_1 SD Data_0
Pin 5 = XDIO_2 SD Command
Pin 7 = XDIO_3 SD Hard Power#
Pin 9 = XDIO_4 SD Data_2
Pin 11 = XDIO_5 SD Data_3
Pin 13 = XDIO_6 SD Clock
Pin 15 = XDIO_7 SD Present#
Pin 14 = XDIO_8 SD Write Prot.

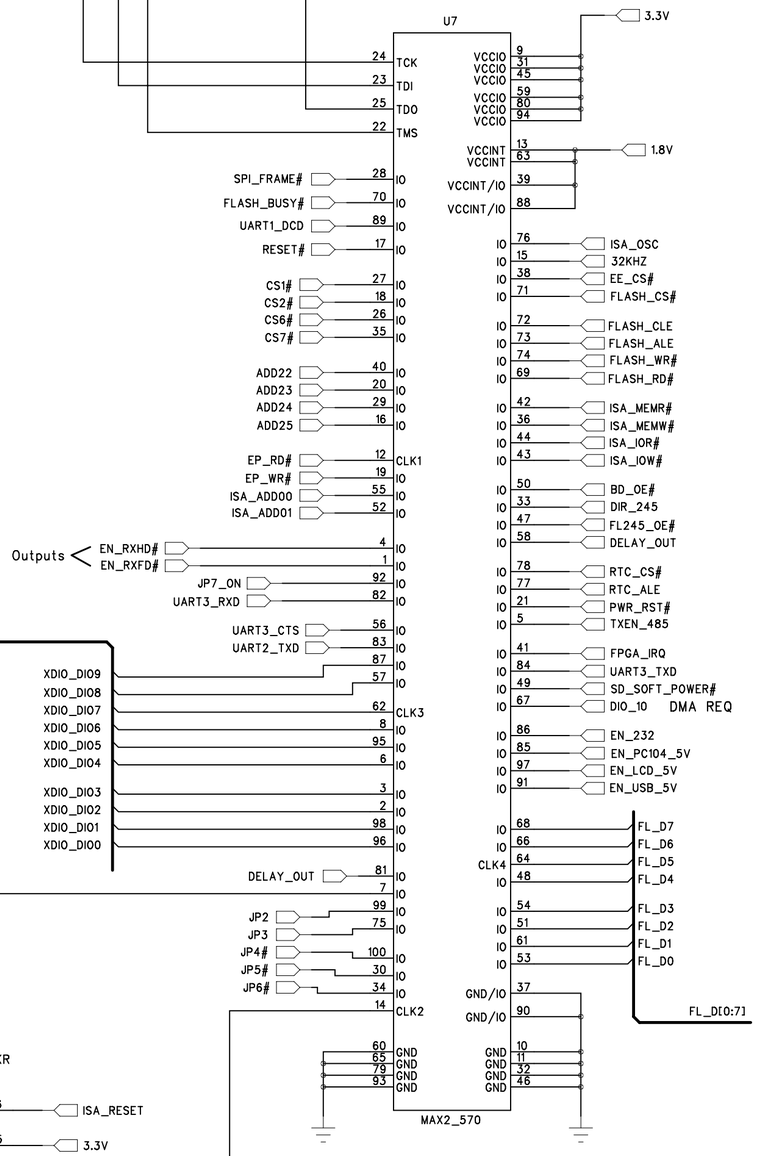
All of these pins need the FPGA pull-up resistor turned on except the SD Clock signal and SD Hard Power# signal

DIO2 Port









Technologic Systems	Date May 20, 2006	
Title: TS-7260 FPGA,		
Rev:	Designer RLM	Sheet 6 of 6